

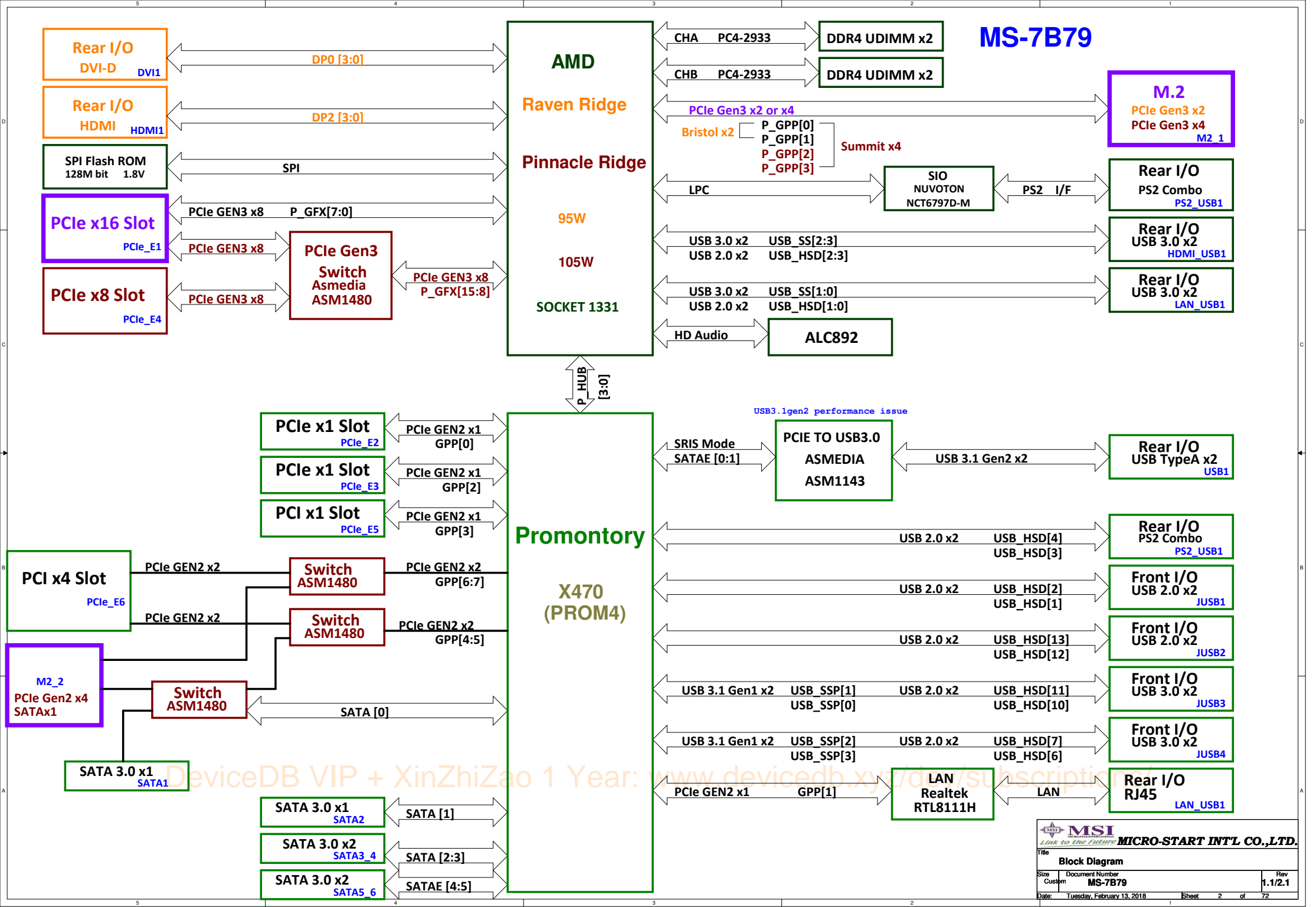
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★

MS-7B79 BOM List			
Schematic Cfg	ERP NO.	Remark	BOM
CFG-7B79-0A-X470-GAMING_PRO	601-7B79-01S		A
CFG-7B79-0A-X470-GAMING_PLUS	601-7B79-02S		

MSI BOM:





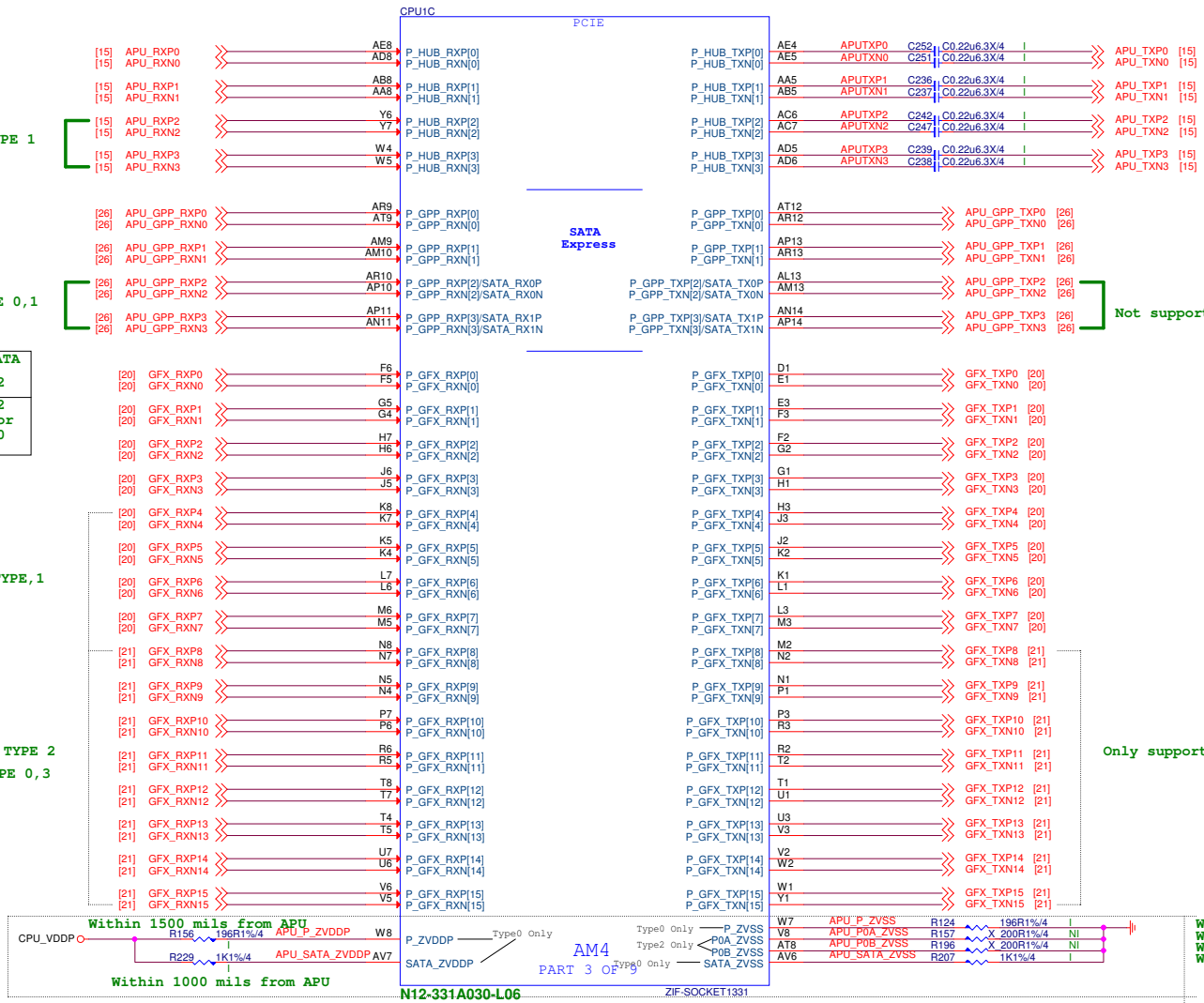
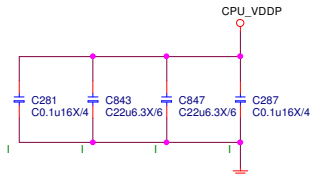
Not supported HUB on TYPE 1

Not supported PCIE on TYPE 0,1

	PCIE	SATA
TYPE 0	2	2
TYPE 2/3	2 or 4	2 or 0

Not supported GFX 4~15 on TYPE,1

Only supported on TYPE 2
Not supported GFX 8~15 on TYPE 0,3




Only supported on TYPE 2

Within 1500 mils from APU
Within 1500 mils from APU
Within 1000 mils from APU
Within 1000 mils from APU

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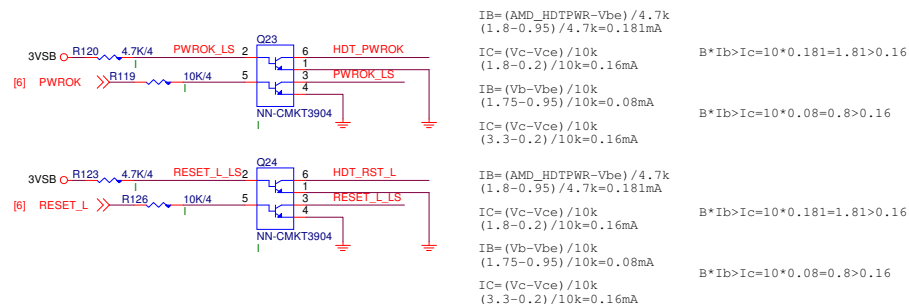
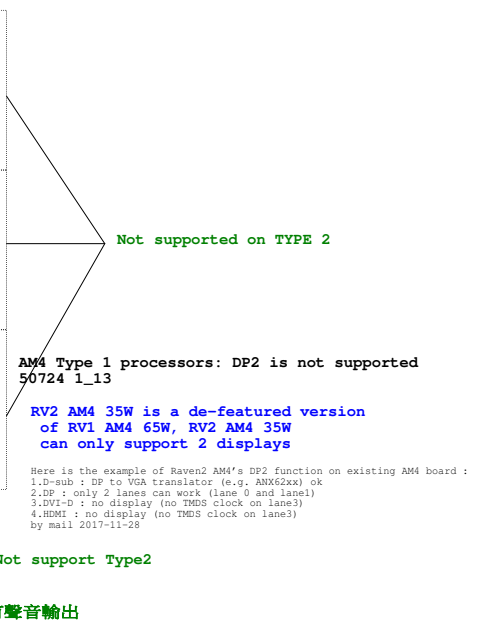
Schematic Cfg	Project
CFG-7B79-0A-X470-GAMING PRO	V A
CFG-7B79-0A-X470-GAMING PLUS	



**MICRO-START INT'L CO.,LTD.**

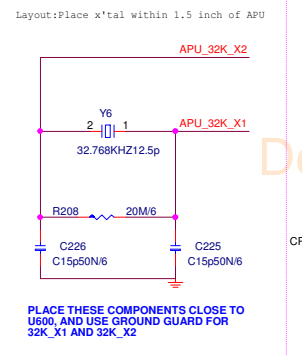
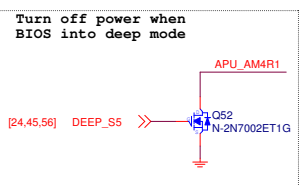
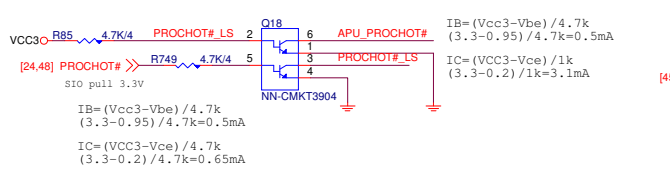
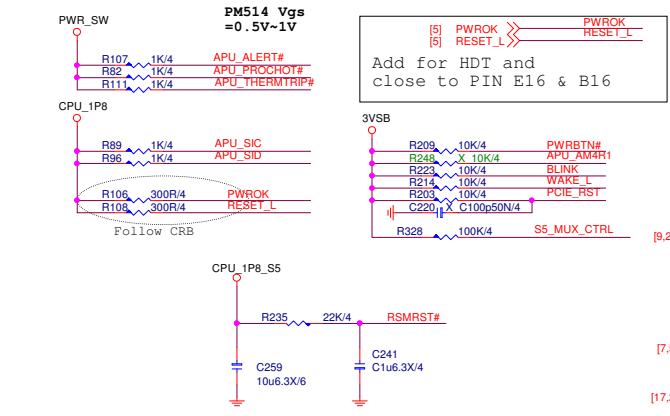
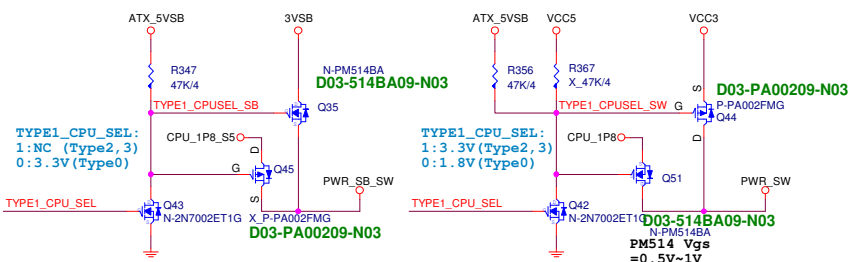
AM4 PCIE/SATAE

Size	Custom	Document Number	Rev
		MS-7B79	1.1/2.1

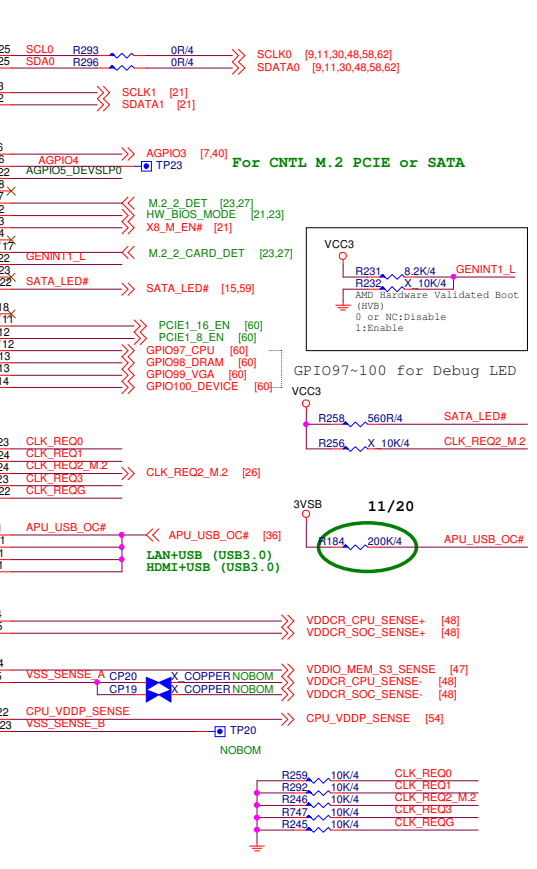
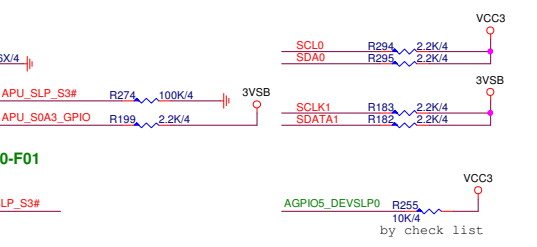
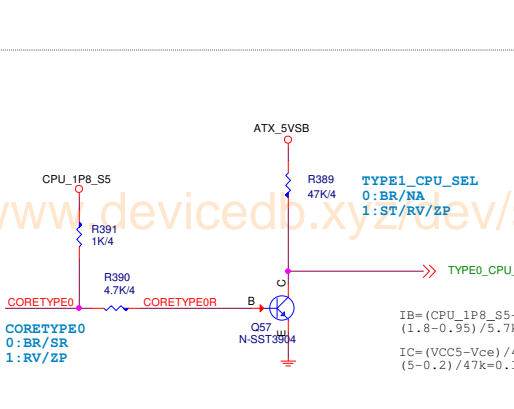
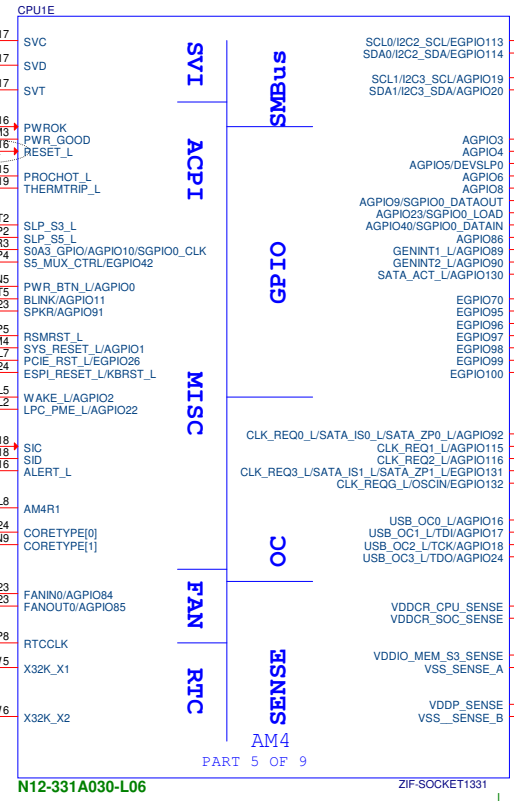
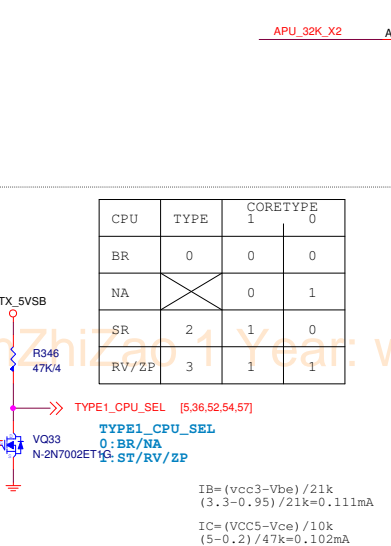
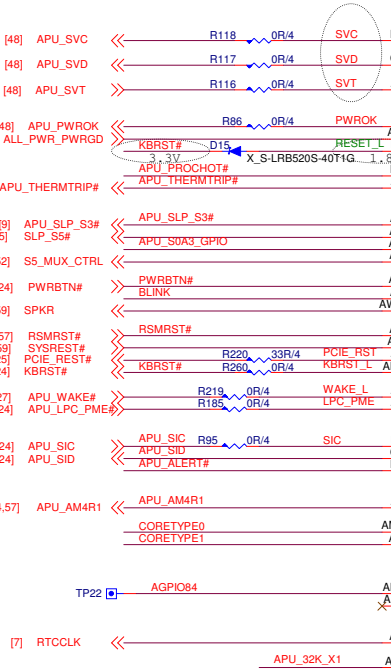
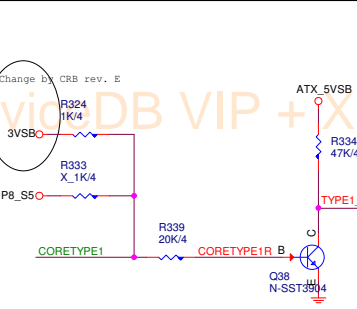
Date:	Tuesday, February 13, 2018	Sheet	4	of	72
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Link to the Future			
MICRO-START INT'L CO.,LTD.			
Title			
AM4 DISPLAY/AUDIO			
Size Custom	Document Number MS-7B79	Rev 1.1/2.1	
Date: Tuesday, February 13, 2018	Sheet 5	of 72	



AM4 CPU TYPE Circuit



MSI

Link to the Future

MICRO-START INT'L CO.,LTD.

Project

CFG-7B79-0A-X470-GAMING PRO

CFG-7B79-0A-X470-GAMING PLUS

Document Number

MS-7B79

Rev

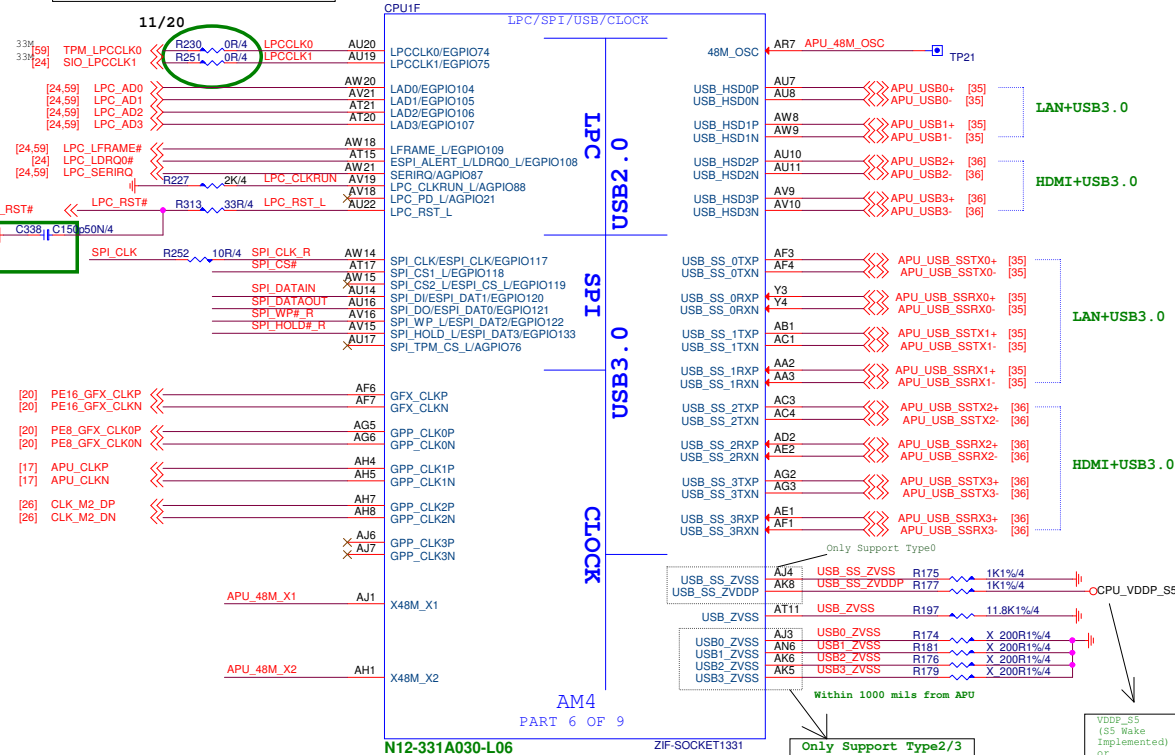
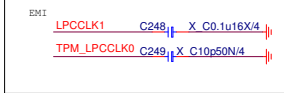
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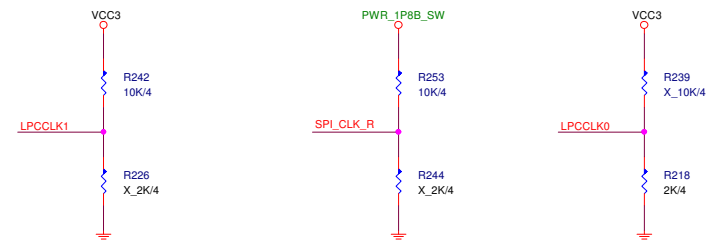
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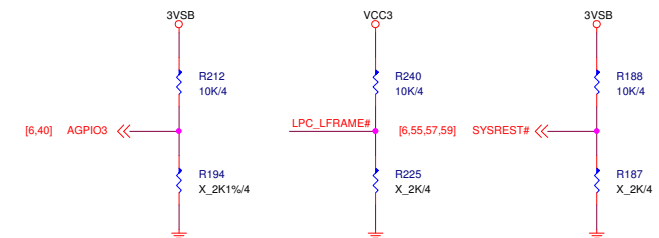
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Strapping Options

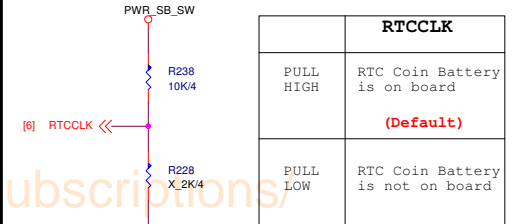
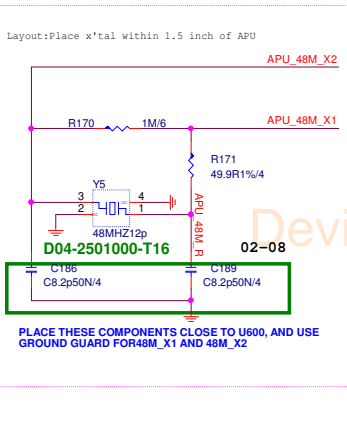
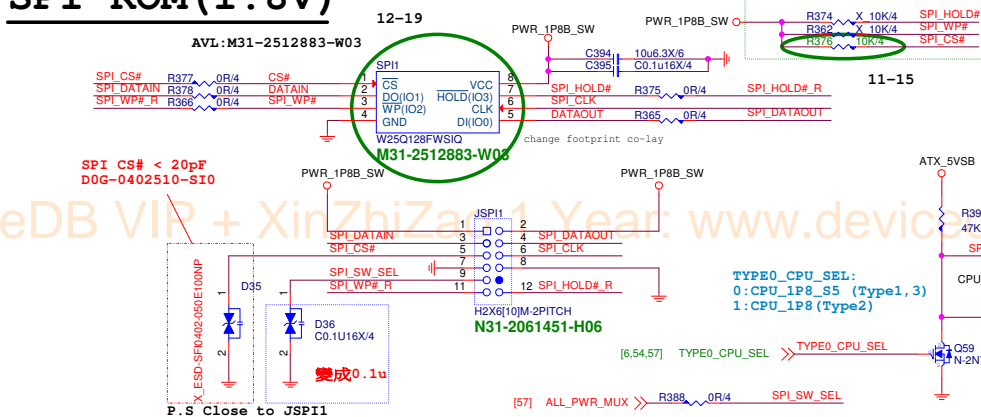


	LPCCLK1	SPI_CLK	LPCCLK0
PULL HIGH	Configured for Internal clock generator (Default)	Use 48Mhz crystal clock and generate both internal and external clocks (Default)	LPC device Boot Fail Timer Enabled
PULL LOW	Configured for External clock generator ?????	Use 100Mhz PCIE clock as reference clock and generate internal clocks only	LPC device Boot Fail Timer Disabled (Default)

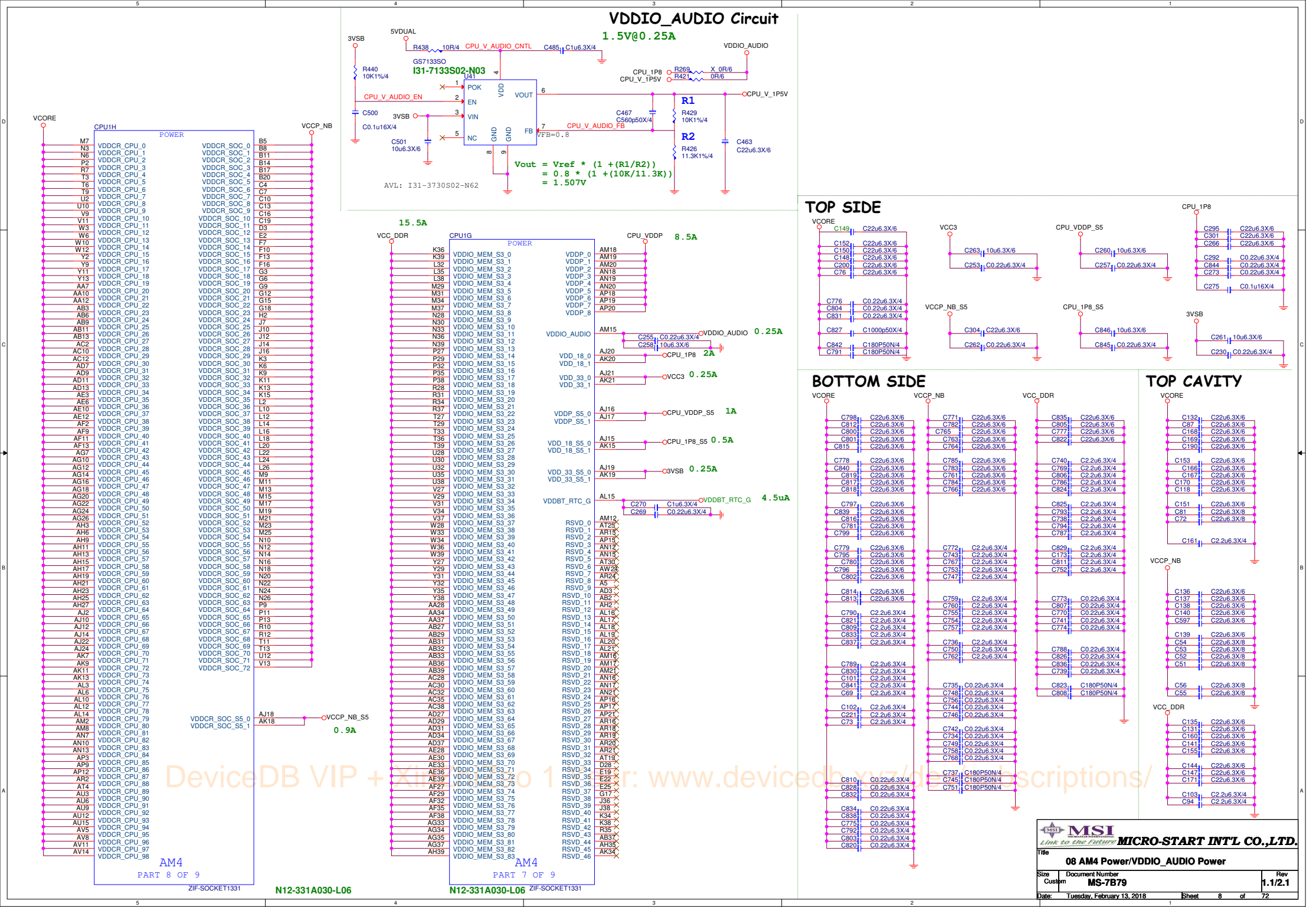


	AGPIO3	SIO_LFRAME	SYSREST#
PULL HIGH	Enhanced Reset logic (Default)	SPI ROM (Default)	Normal reset mode (Default)
PULL LOW	Traditional Reset logic	LPC ROM	short reset mode

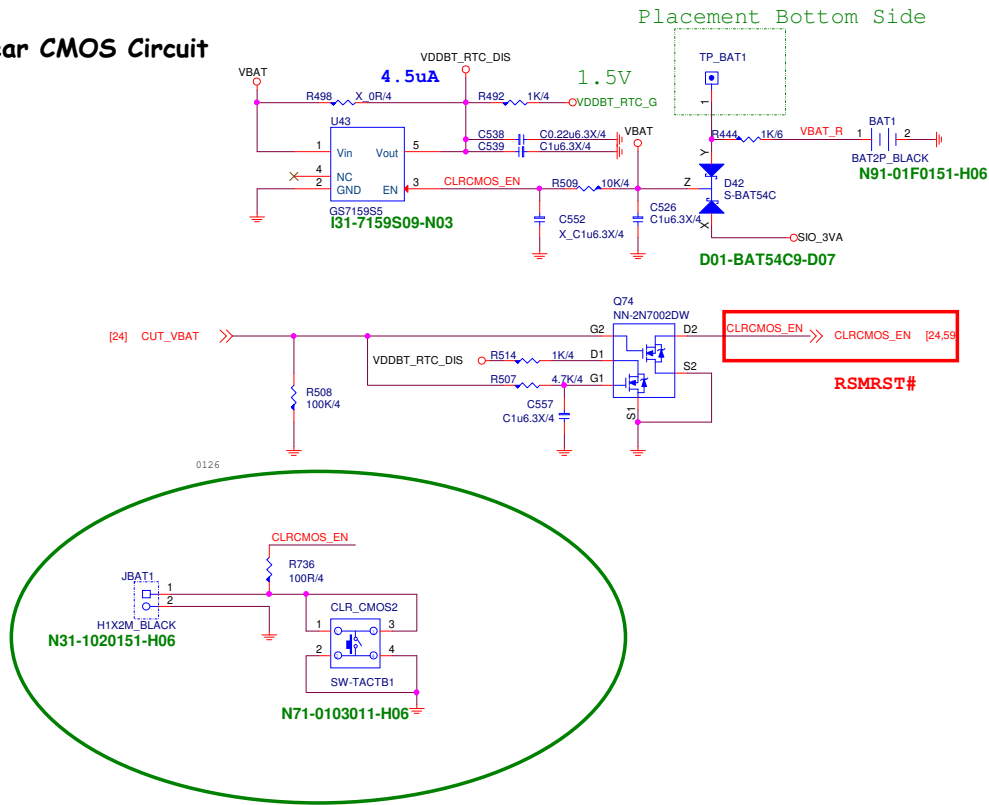
SPI ROM (1.8V)



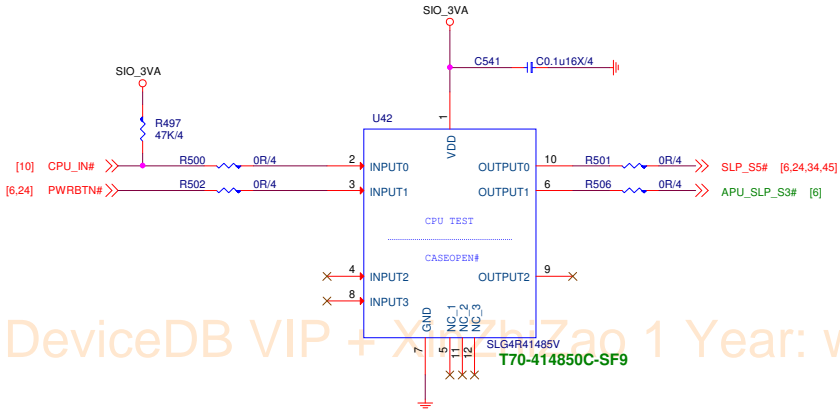
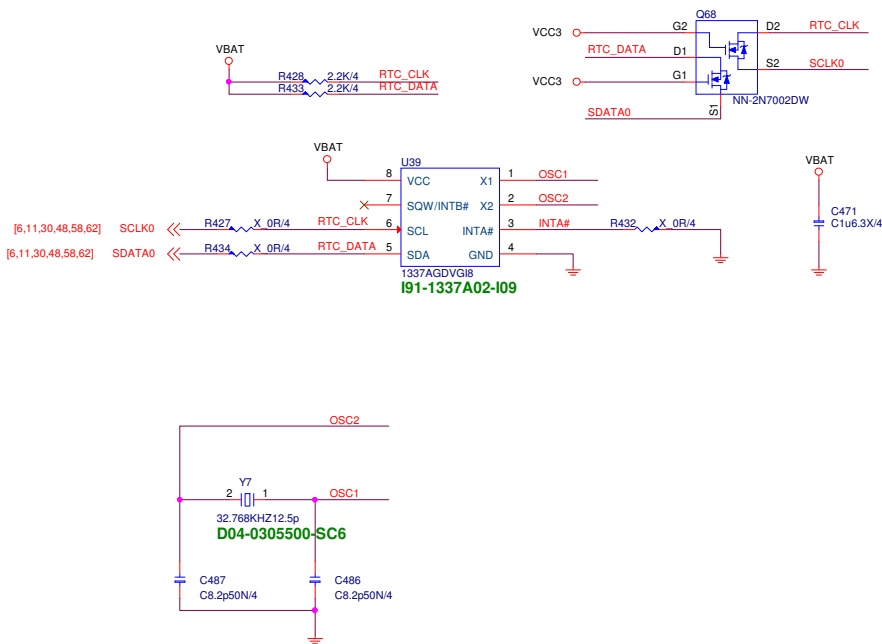
	RTCCLK
PULL HIGH	RTC Coin Battery is on board (Default)
PULL LOW	RTC Coin Battery is not on board



RTC & Clear CMOS Circuit



RTC Backup



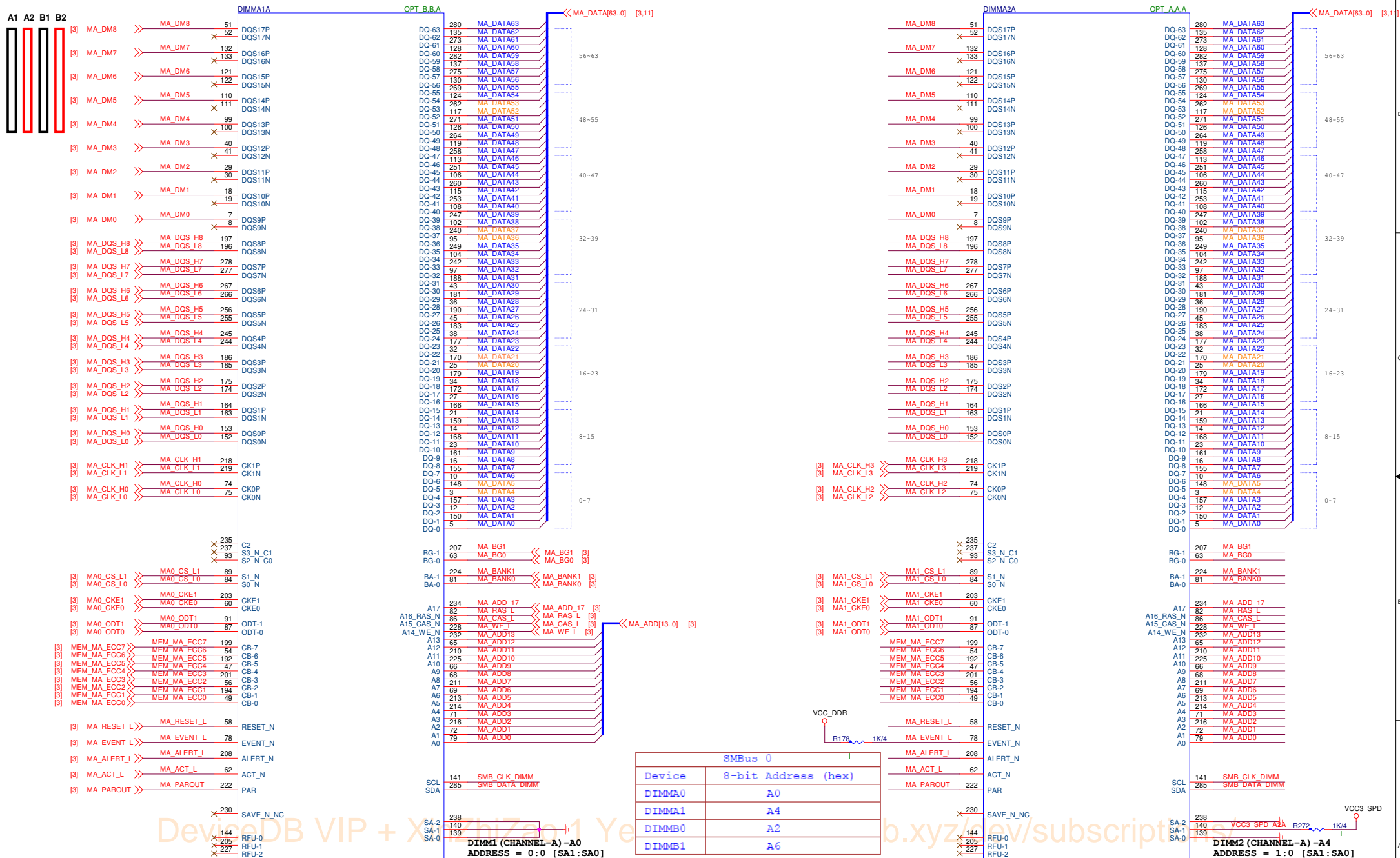
Function 2				
IN		OUT		
INPUT3 & lowswitch EN	INPUT4	OUTPUT2	OUTPUT3	VOUT
0	0	0	1	1
1	0	1	1	0 (discharge)
0	1	1	0	0 (discharge)
1	1	1	0	0 (discharge)

Default

GND

AM4
PART 9 OF 9


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DDRIV-288P
N13-2880581-L06

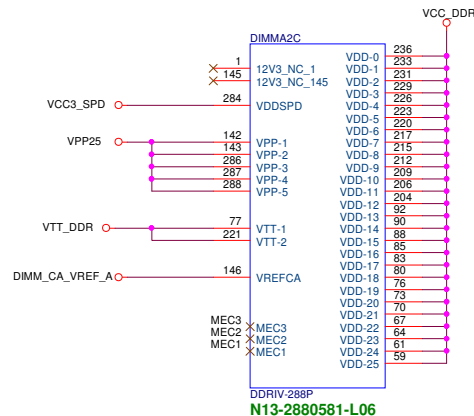
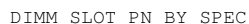
DDRIV-288P
N13-2880581-L06

Schematic Cfg		Project	
CFG-7B79-0A-X470-GAMING PRO		V	A
CFG-7B79-0A-X470-GAMING PLUS			

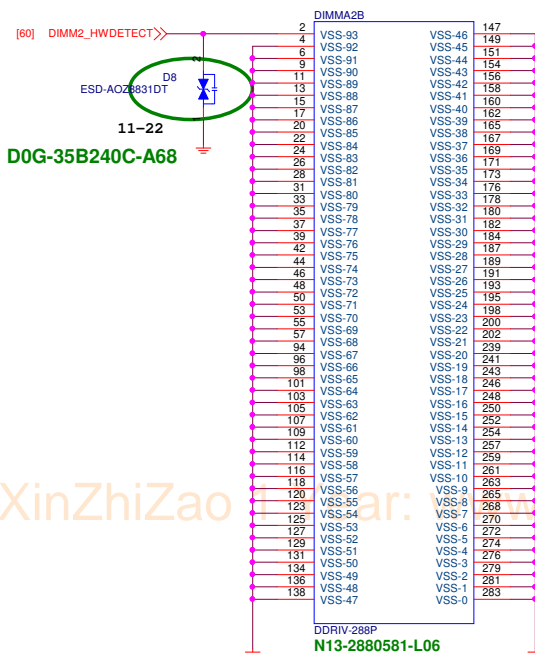
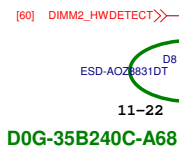
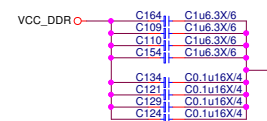
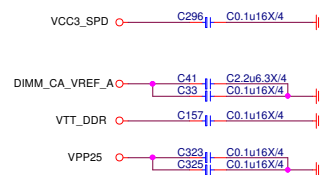
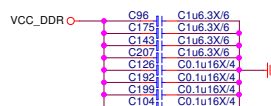
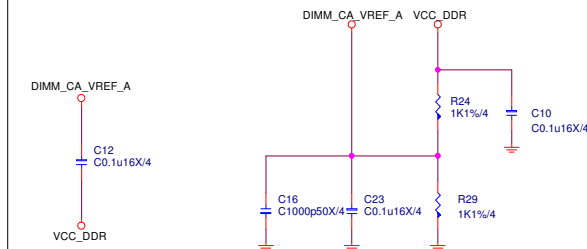
 MSI MICRO-STAR INTERNATIONAL <i>Link to the Future</i>		MICRO-START INT'L CO.,LTD.	
Title			
DDR4 DIMM CH-A			
Size	Document Number	Rev	
Custom	MS-7B79	1.1/2.1	
Date:	Tuesday, February 13, 2018	Sheet	11 of 72

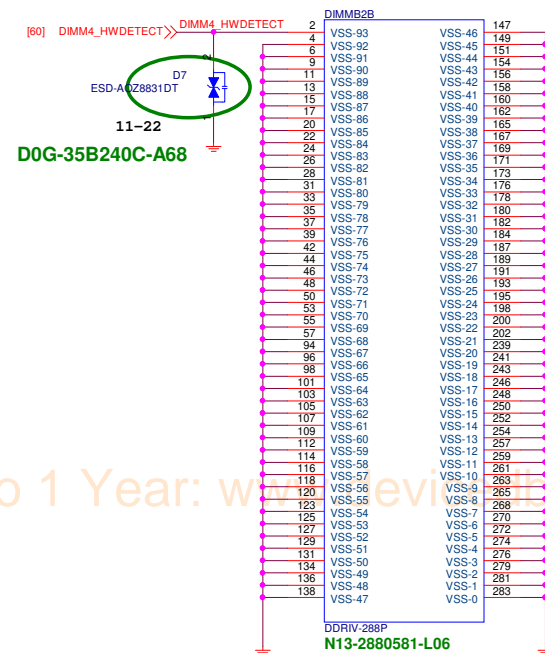
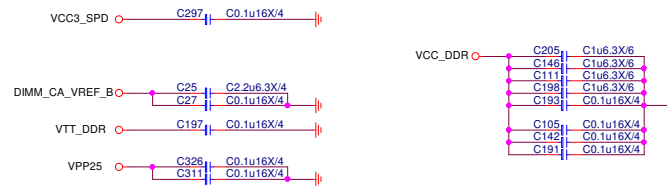
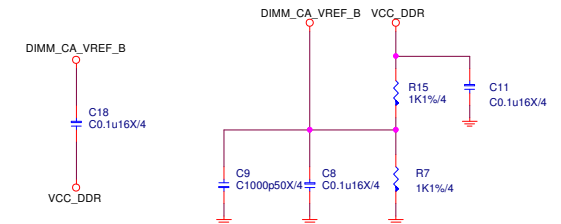
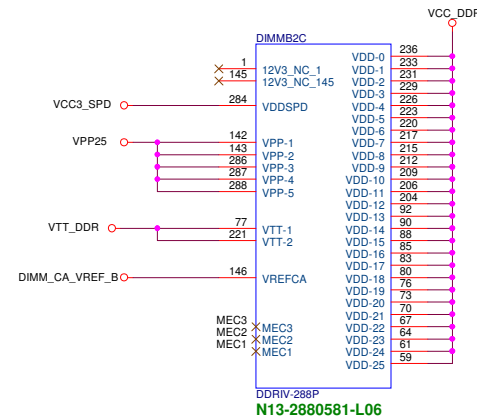
[6,9,30,48,58,62] SCLK0 R297 0R/4 SMB_CLK_DIMM SMB_CLK_DIMM [12]
[6,9,30,48,58,62] SDATA0 R298 0R/4 SMB_DATA_DIMM SMB_DATA_DIMM [12]

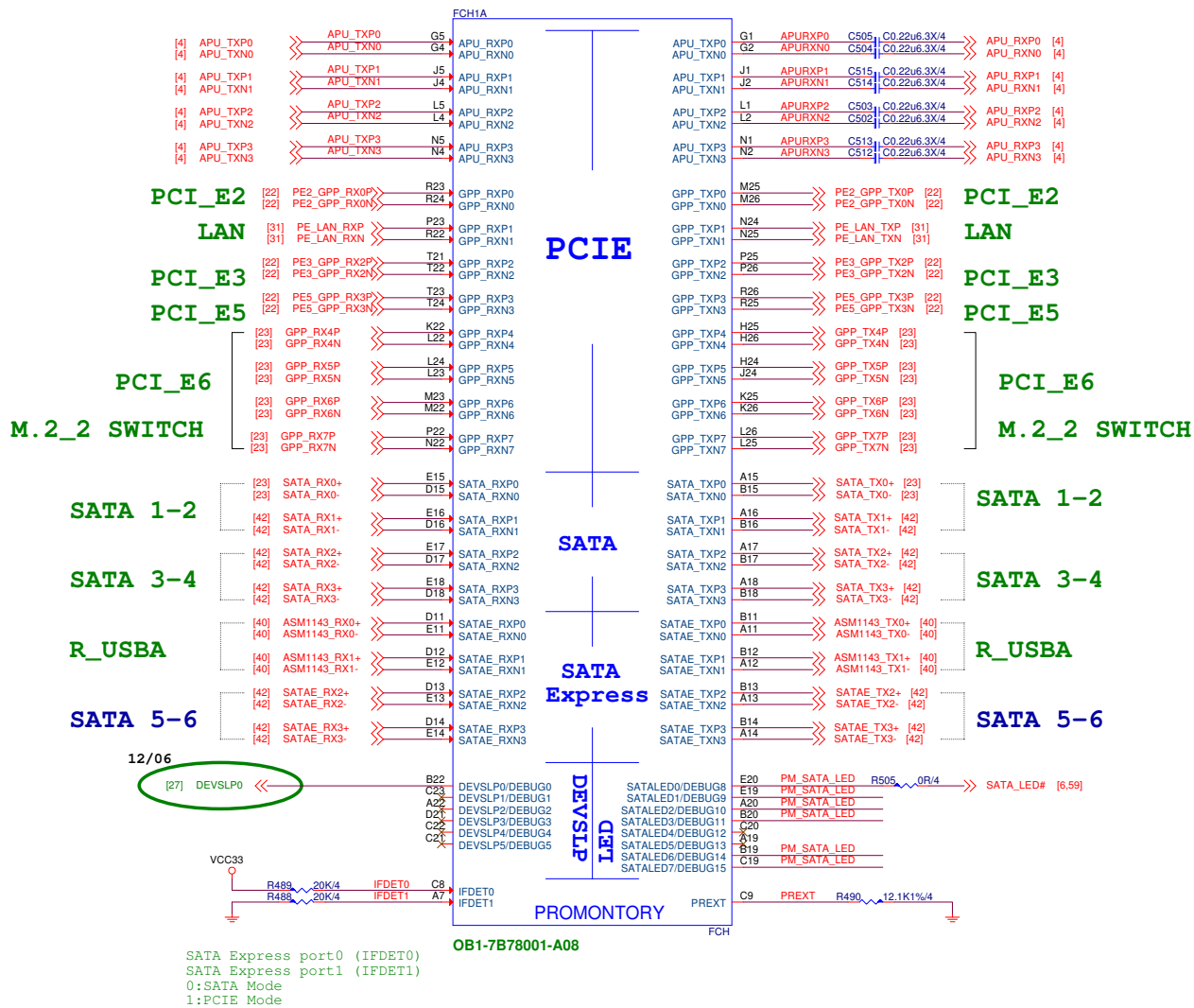
VCC3 1  2 VCC3_SPD
F10
F-SPR-P260T
D08-0301000-P16



(place resistors close to DIMMs)







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Appendix D USB Port to OC Pin Mapping

USB3.1	USB2.0	USB_OC
USB_SSP_TX/RXP/N[0]	USB_HSDP/N[5]	USB_OC0N
USB_SSP_TX/RXP/N[1]	USB_HSDP/N[0]	USB_OC1N
USB3.0	USB2.0	USB_OC
USB_SS_TX/RXP/N[0]	USB_HSDP/N[10]	USB_OC2N
USB_SS_TX/RXP/N[1]	USB_HSDP/N[11]	USB_OC3N
USB_SS_TX/RXP/N[2]	USB_HSDP/N[6]	USB_OC4N
USB_SS_TX/RXP/N[3]	USB_HSDP/N[7]	USB_OC5N
USB_SS_TX/RXP/N[4]	USB_HSDP/N[8]	USB_OC6N
USB_SS_TX/RXP/N[5]	USB_HSDP/N[9]	USB_OC7N
	USB_HSDP/N[1]	USB_OC7N
	USB_HSDP/N[2]	USB_OC7N
	USB_HSDP/N[3]	USB_OC7N
	USB_HSDP/N[4]	USB_OC7N
	USB_HSDP/N[12]	USB_OC7N
	USB_HSDP/N[13]	USB_OC7N


Appendix C Port Mapping for Different Bus Models

BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0~1	USB_SS Port 0~5	USB_HSD Port0~13	USB_SSP Port0
PROM2	USB_SSP Port0~1	USB_SS Port 0~1	USB_HSD Port0~5 USB_HSD Port10~13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port1	USB_HSD Port0~5 USB_HSD Port10, 12~13	USB_SSP Port0

BUS Model	SATA 3.0	SATA Express	PCI Express® Gen2 GPP	PCI Express® CLK
PROM4	SATA port0~3	SATAE port0~3	GPP lane0~7	CLK0~7
PROM2	SATA port0~1	SATAE port0~1	GPP lane0~1 GPP lane4~7	CLK0~1 CLK4~7
PROM1	SATA port0~1	SATAE port0~1	GPP lane4~7	CLK4~7

CLK2.3不能
CLK1-3不能

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MICRO-START INT'L CO.,LTD.

Title

Promontory-USB/OC

Size

Custom

Document Number

MS-7B79

Rev

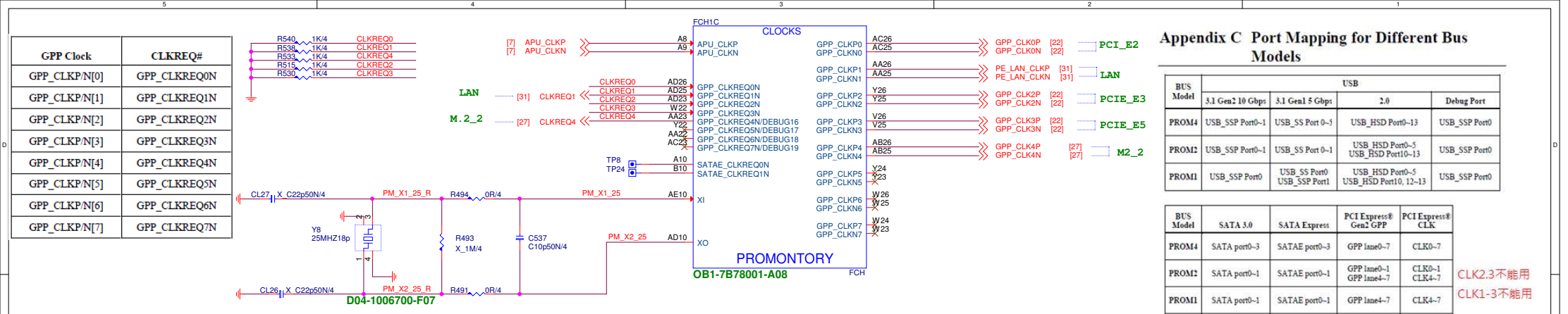
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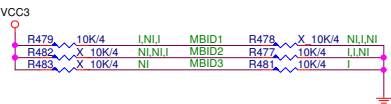
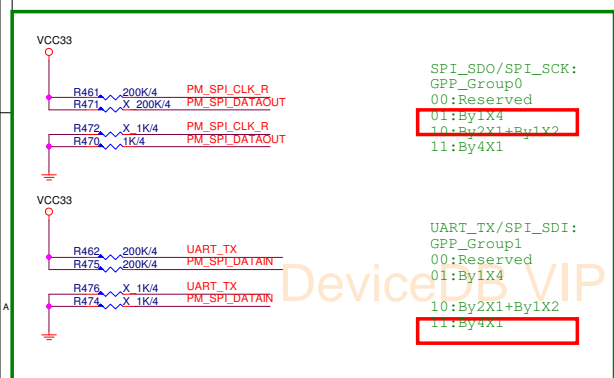
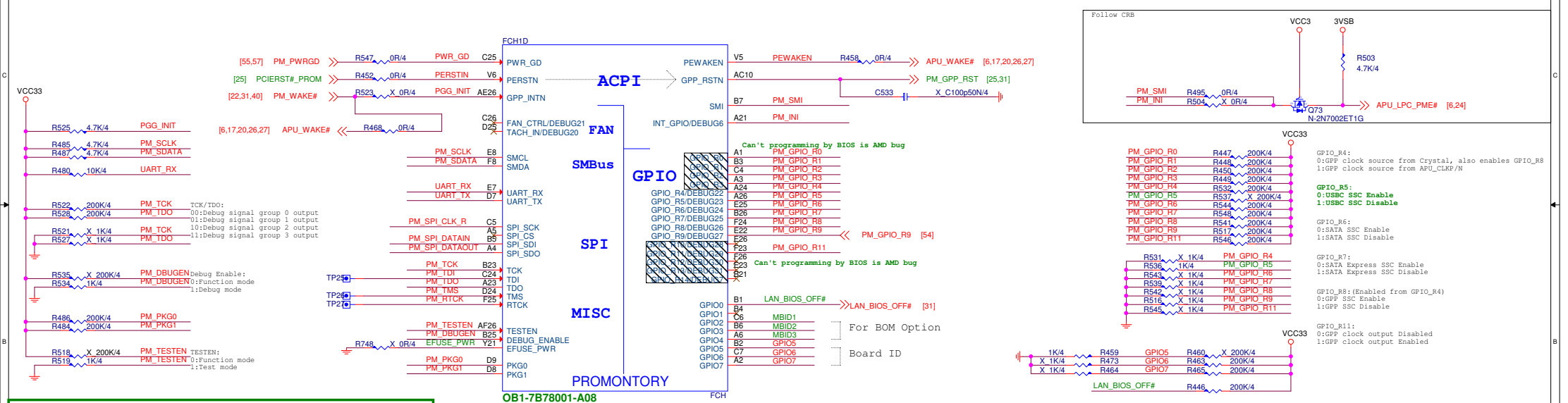
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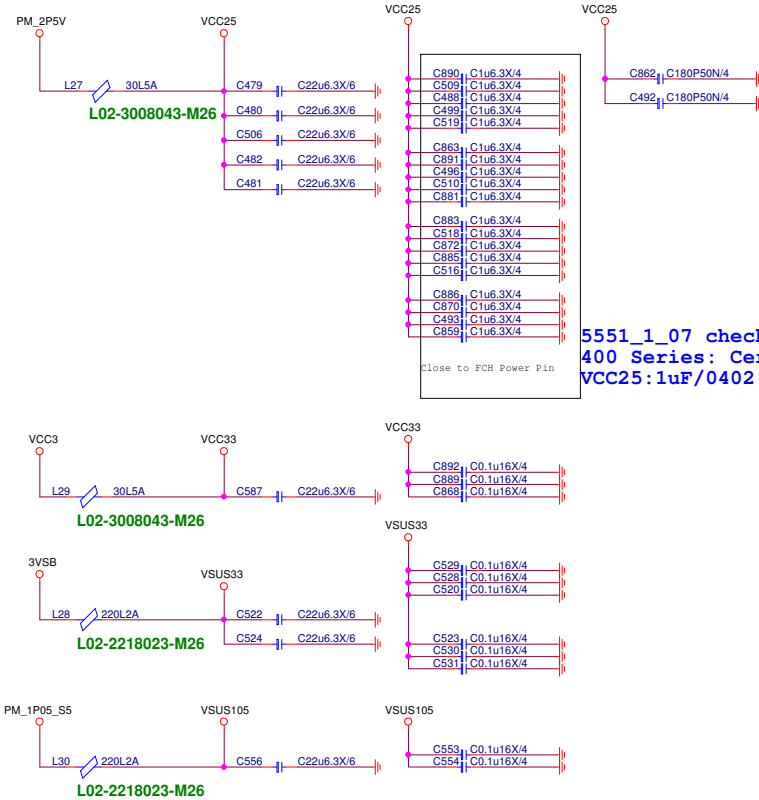
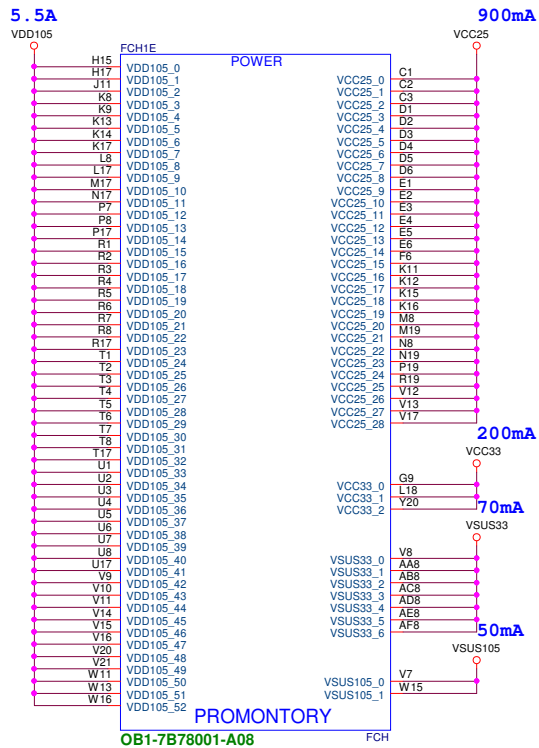
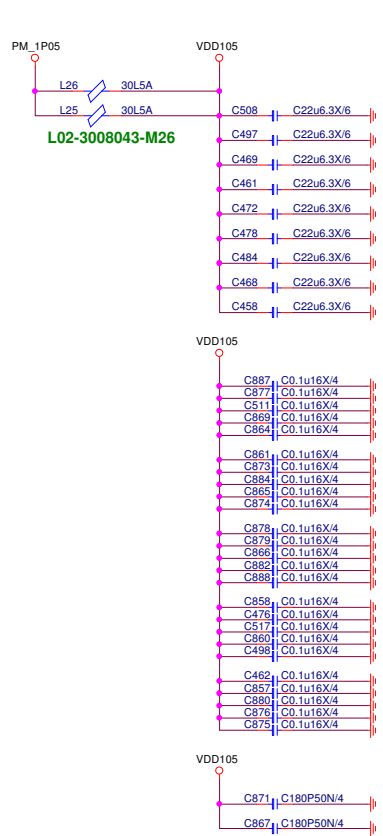
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BUS Model	USB			
	3.1 Gen2 10 Gbps	3.1 Gen1 5 Gbps	2.0	Debug Port
PROM4	USB_SSP Port0-1	USB_SS Port 0-5	USB_HSD Port0-13	USB_SSP Port0
PROM2	USB_SSP Port0-1	USB_SS Port 0-1	USB_HSD Port0-5 USB_HSD Port10-13	USB_SSP Port0
PROM1	USB_SSP Port0	USB_SS Port0 USB_SSP Port0	USB_HSD Port0-5 USB_HSD Port 0, 12-13	USB_SSP Port0



Schematic Cfg	Project	
CFG-7B79-0A-X470-GAMING PRO	V	A
CFG-7B79-0A-X470-GAMING PLUS		

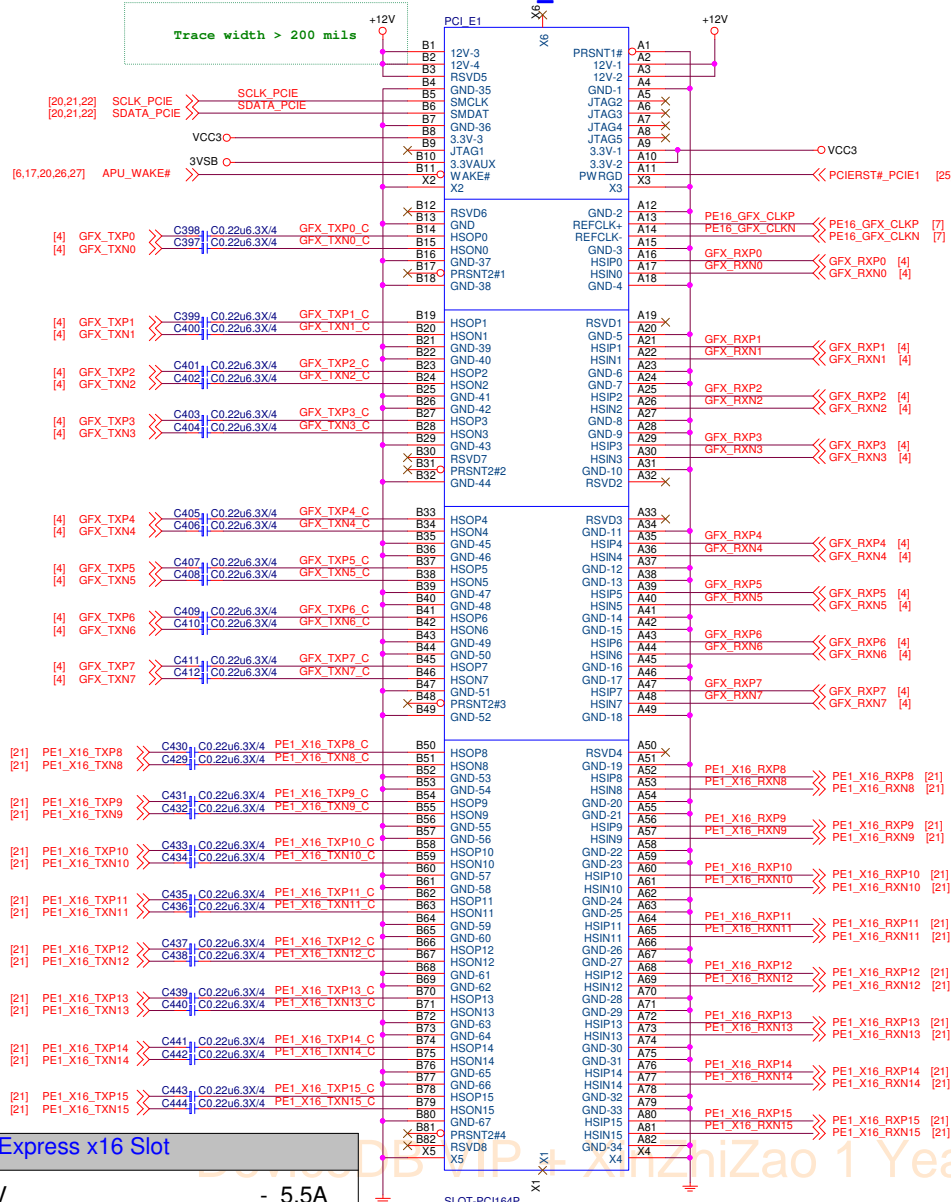


5551_1_07 check list
400 Series: Ceramic capacitors.
VCC25:1uF/0402

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PCI EXPRESS x16 Slot

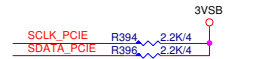
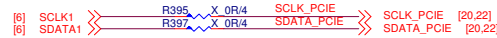
PCI E1



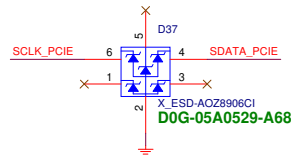
PCI EXPRESS Switch

For PCIE_2 & PCIE_4 (X16/ X8)

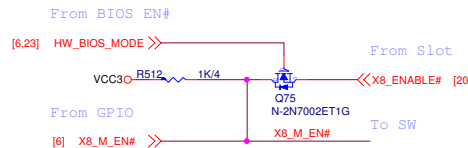
SMBus separate circuit



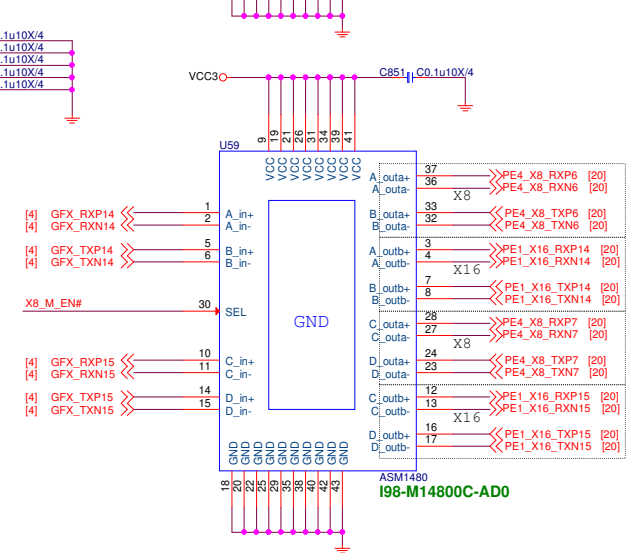
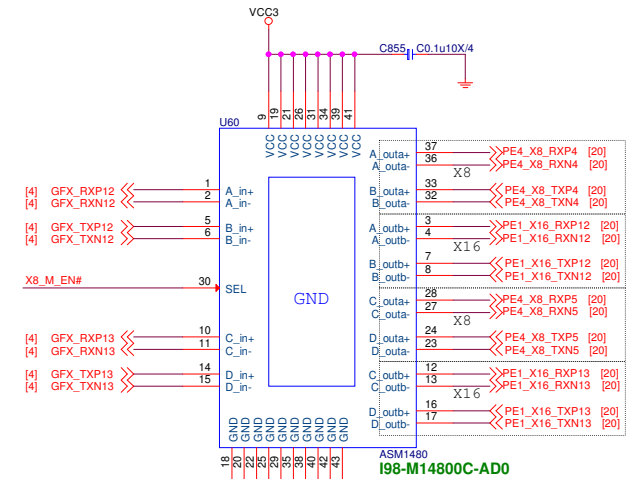
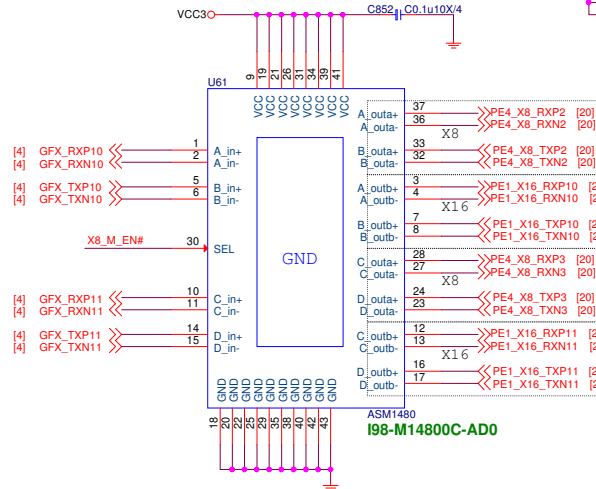
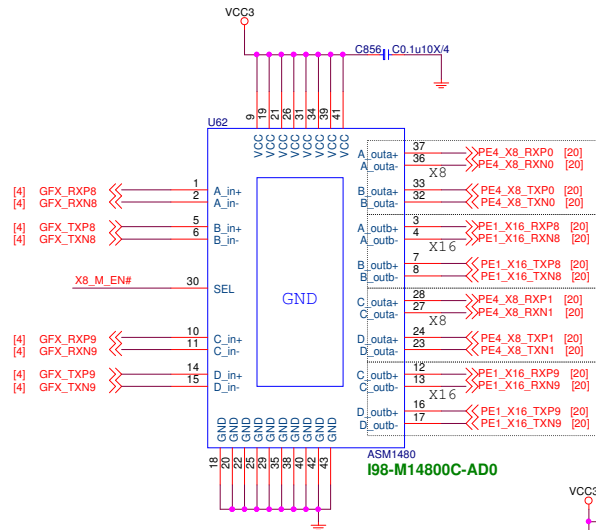
SMB_SEL
GPIO Default High



PCIE Lanes control circuit



	HW_BIOS_MODE	X8_M_EN#
Auto	1	1
Manual x16	0	1
Manual x8, x8	0	0

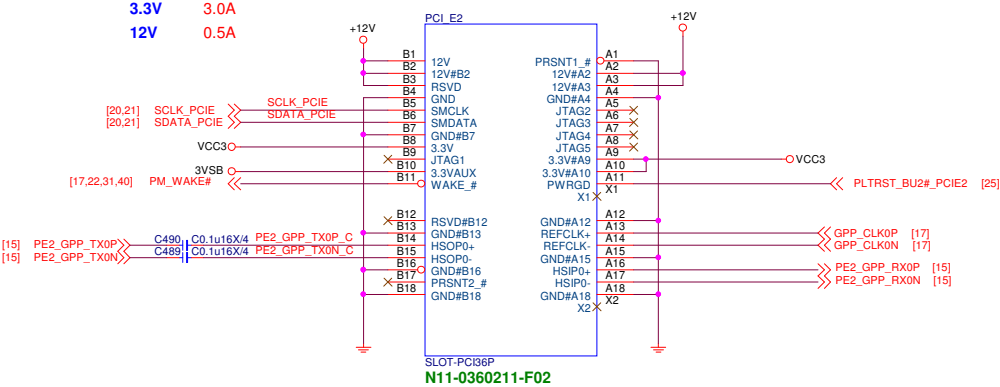


SEL	Function
L	N_in +/1 to N_out+/-
H	N_in +/1 to N_out+/-

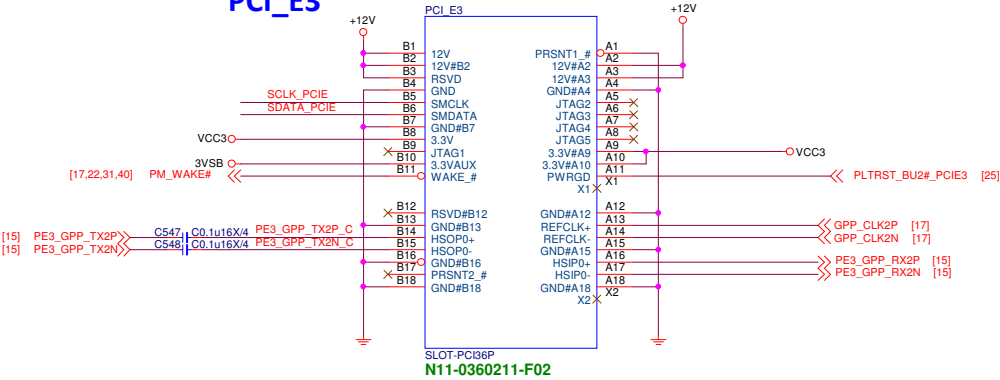
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PCIEX1 12V 0.5A
3.3V weak 375mA

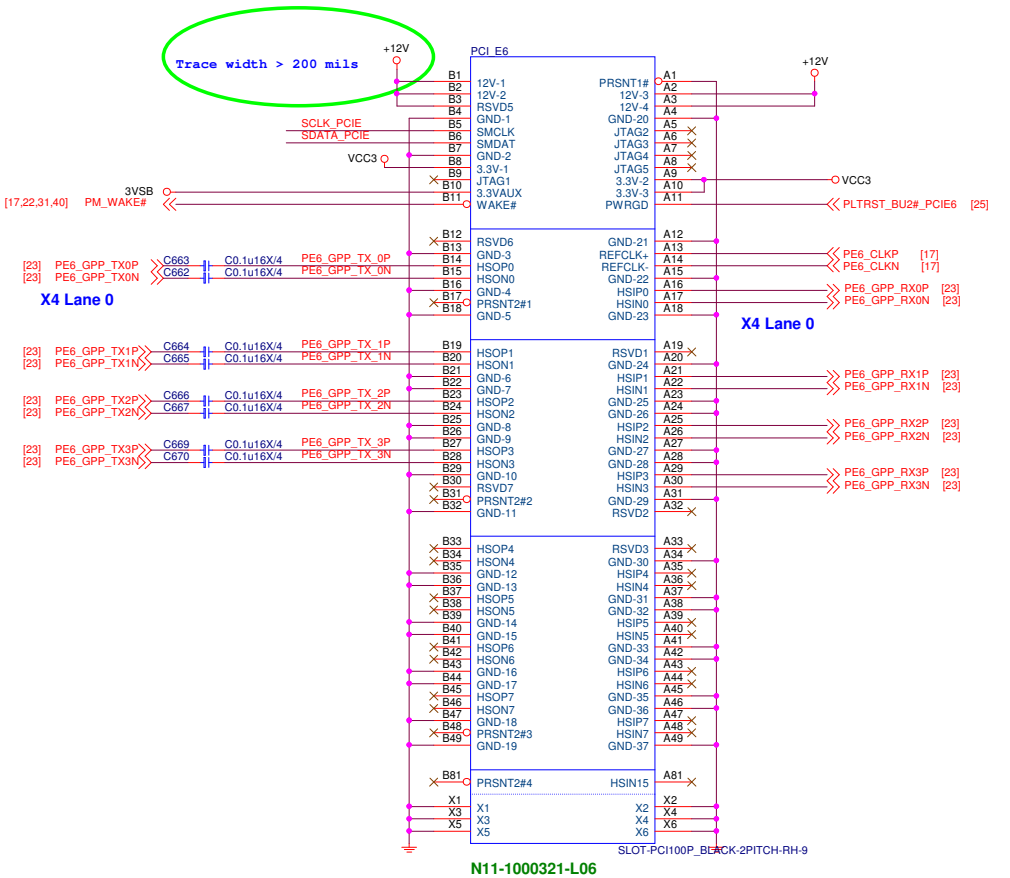
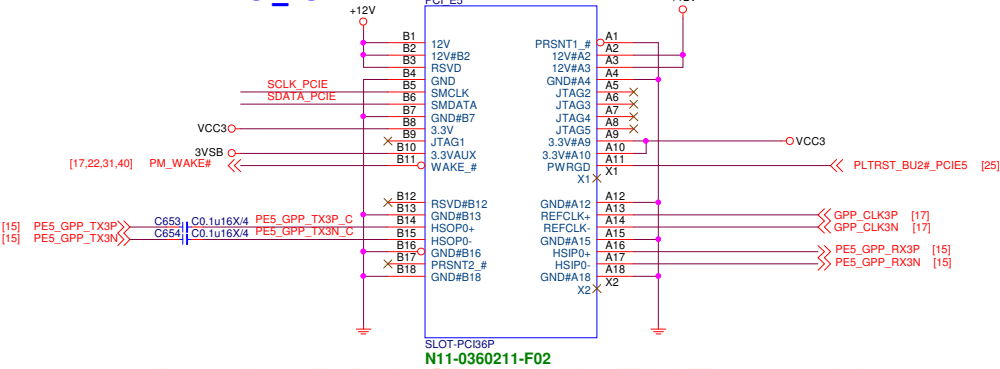
PCI_E2



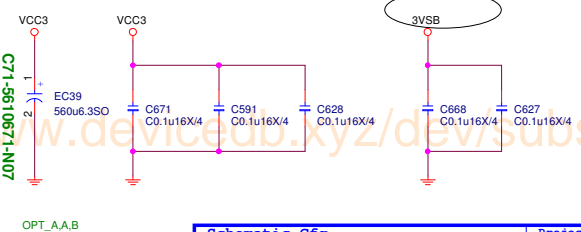
PCI_E3




PCI_E5



PCI Express x4 Slot *1	
+12V	- 2.1A
+VCC3	- 3A
+3V3_S5 (wake)	- 375mA
+3V3_S5 (no wake)	- 20mA
PCI Express x1 Slot *3	
+12V	- 1.5 A
+VCC3	- 9A
+3V3_S5 (wake)	- 1125mA
+3V3_S5 (no wake)	- 60mA



Schematic Cfg		Project	
CFG-7B79-0A-X470-GAMING PRO		V	A
CFG-7B79-0A-X470-GAMING PLUS			

**MICRO-START INT'L CO.,LTD.**

PCI E2_E3_E5/E4 X1/X4

Size

Document Number

Rev

MS-7B79

1.1/2.1

Date:

Tuesday, February 13, 2018

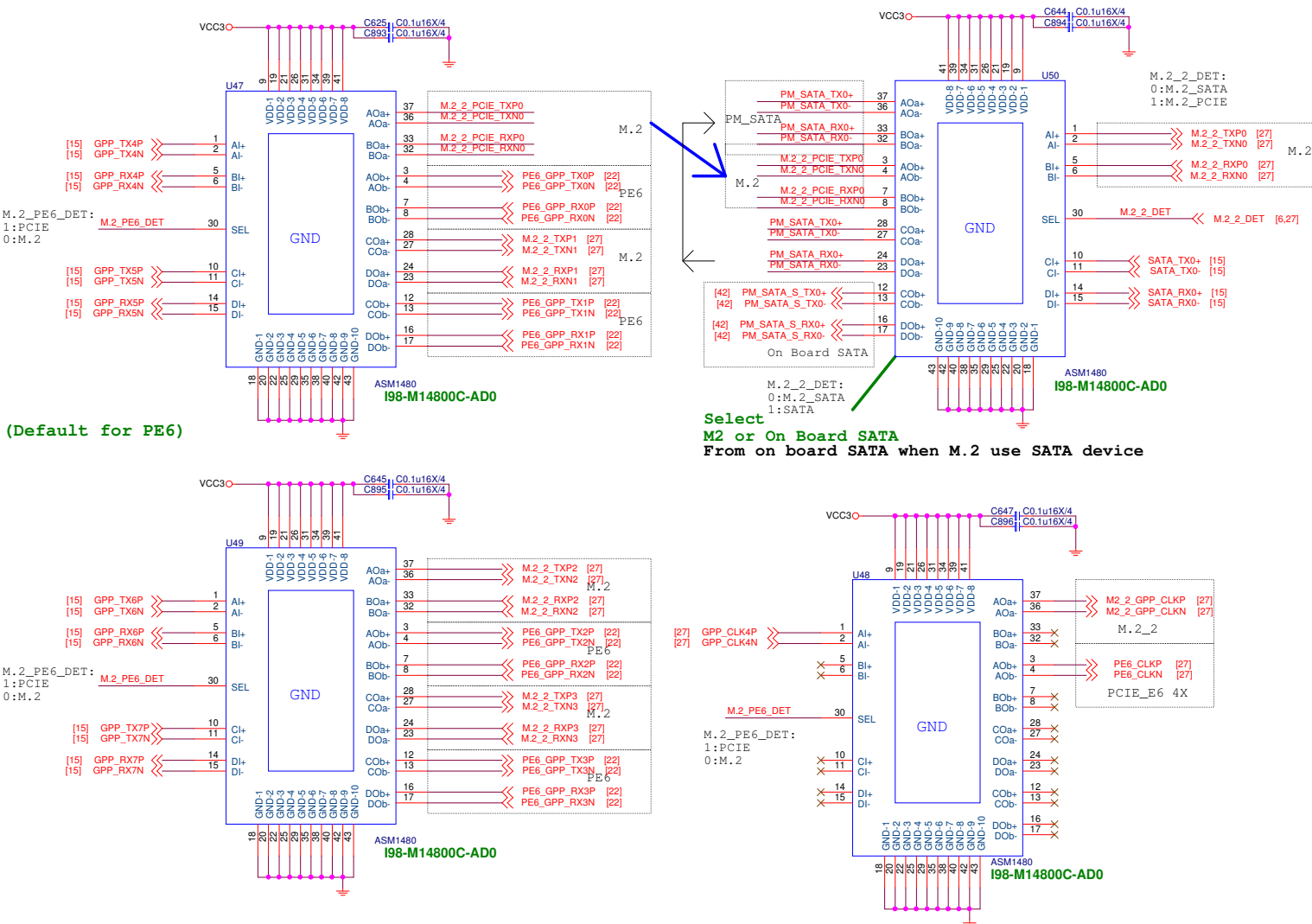
Sheet

22

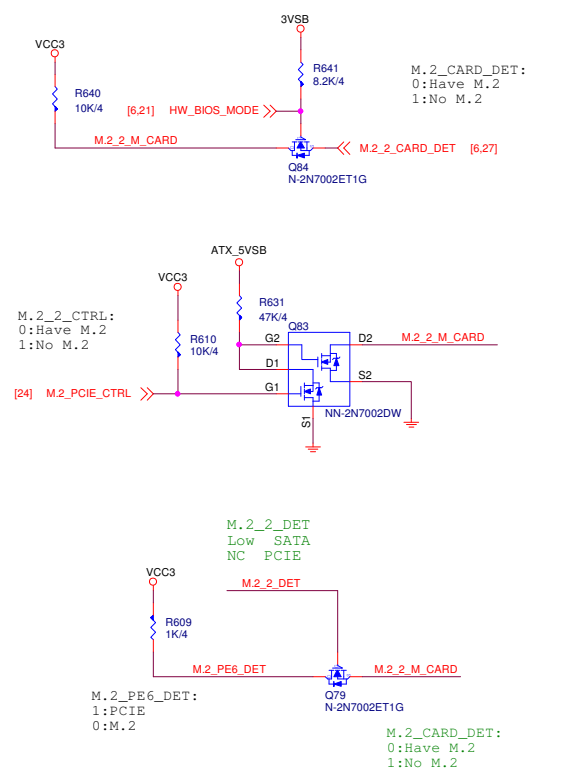
of

72

PCI_E6 and M2_2 and SATA1 Switch




	AUTO Mode	PCIE_x4	M.2 (PCIE)	M.2 (SATA)	SATA CON
HW_BIOS_MODE	1	0	0	0	
M.2_PCIE_CTRL	0	1	0	0	
M.2_2_CARD_DET		1	0	0	1
M.2_DET			1	0	1



DeviceDB VIP + XinZhiZao 1 Year: www.device-db.xyz/dev/subscriptions/

SEL	Function
L	N_in +/1 to N_outa+/-
H	N_in +/1 to N_outb+/-

**MICRO-START INT'L CO.,LTD.**

PCIE Switch X4 / M2_2

Size Custom

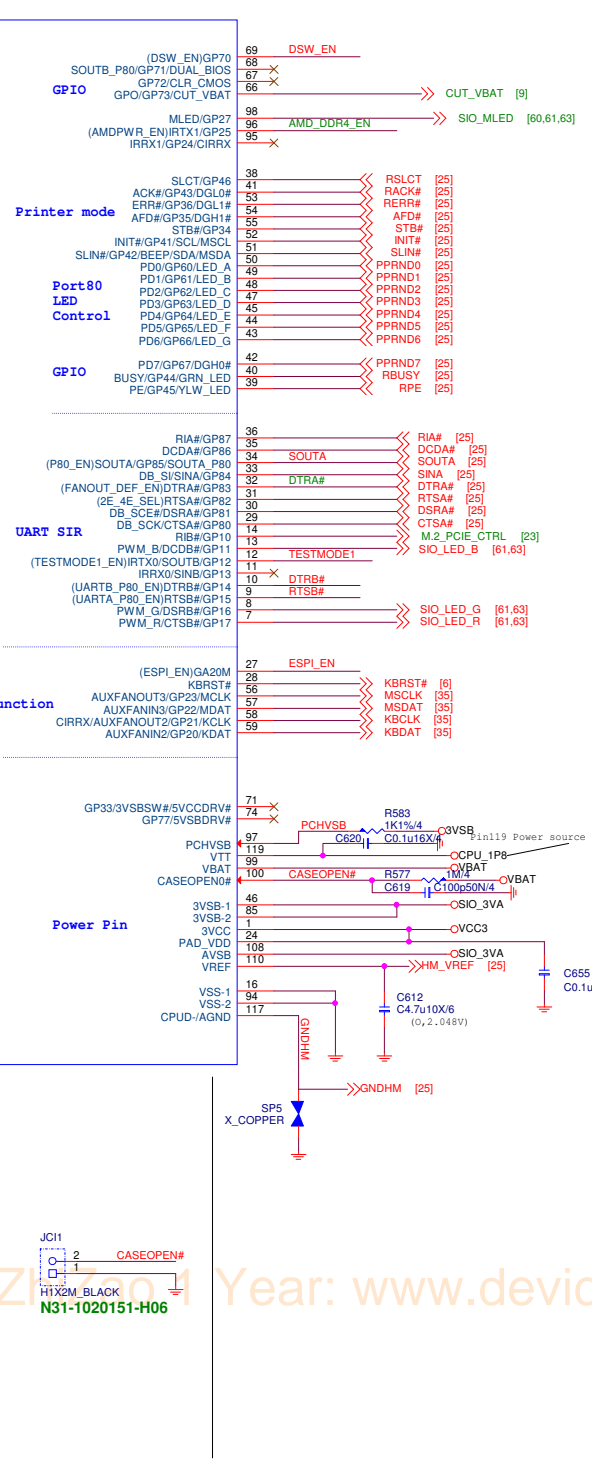
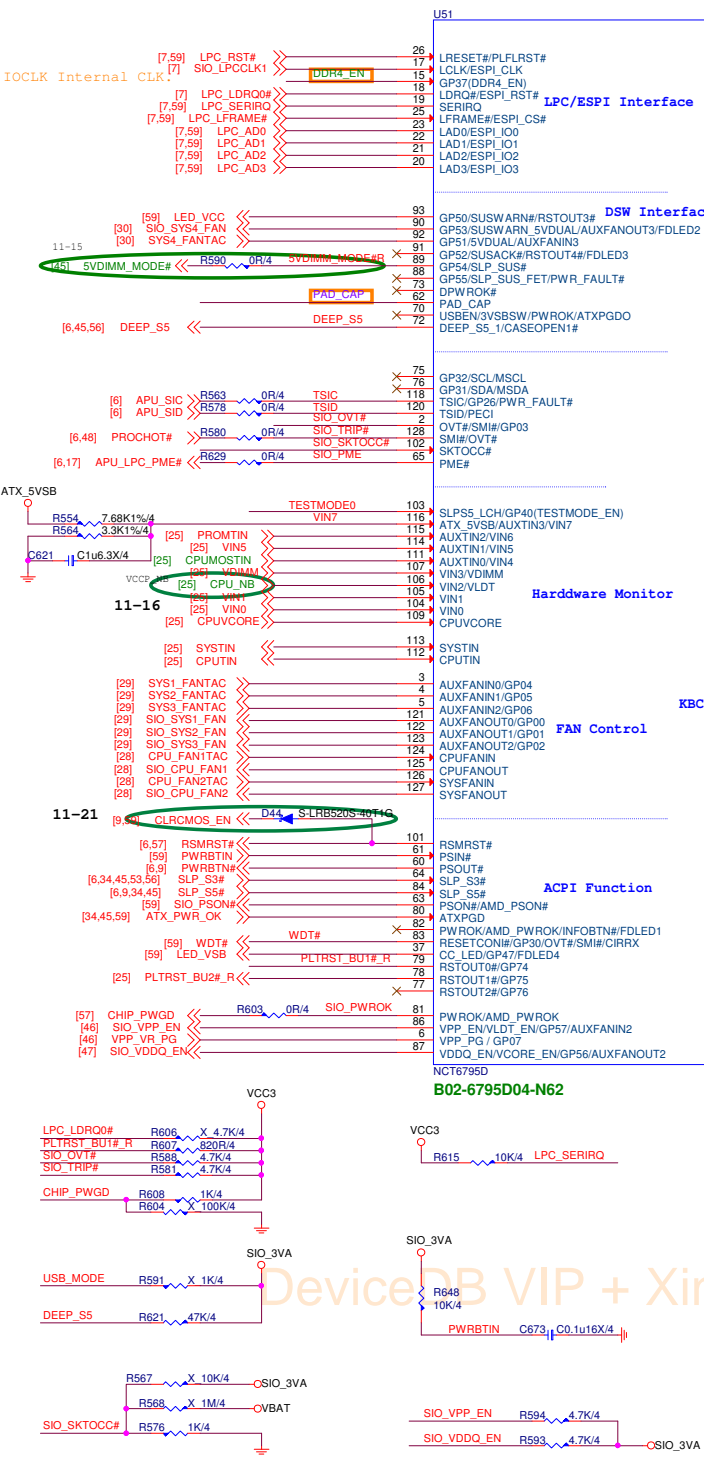
Document Number

MS-7B79

Date: Tuesday, February 13, 2018

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Rev 1.1/2.1



POWER ON STRAPPING PIN FOR NCT6797/6795

PIN	6797/6795 NAME	Circuit NAME	0	1	Strap Point
9	UARTA_P80_EN	RTSB#	DISABLE UARTA80	ENABLE UARTA80	LRESET
10	UARTB_P80_EN	DTRB#	DISABLE UARTB80	ENABLE UARTB80	LRESET
12	TESTMODE1_EN	TESTMODE1_EN	DISABLE TEST1MODE	ENABLE TEST1MODE	LRESET
15	DDR4_EN	DDR4_EN	Disable	Enable	
27	ESPI_EN	ESPI_EN	LPC	ESPI	
31	2E_4E_SEL	RTSA#	I/O ADDRESS 2E	I/O ADDRESS 4E	LRESET
32	FANOUT_DEF_EN	DTRA#	default 50%	default 100%	INTERNAL PWROK
34	P80_EN	SOUTA	ENABLE Non_PORT80	ENABLE PORT80	LRESET
69	DSW_EN	DSW_EN	DISABLE INTEL DSW	ENABLE INTEL DSW	INTERNAL RSMRST
96	AMDPWR_EN	AMDPWR_EN	DISABLE AMD PWR SEQ	ENABLE AMD PWR SEQ	INTERNAL RSMRST
103	6795 TESTMODE_EN 6797 GP40	6795 WDT# 6797 WDT#	6795 DISABLE TESTMODE	6795 ENABLE TESTMODE	INTERNAL RSMRST

Note:
If PIN34 strapping low, BIOS must programming LPT or GPIO

DTRA# high FAN 100% LOW FAN 50%

3V Analog Power

Closed PIN108

Closed PIN99

Closed PIN1,24

Closed PIN46,85

DeviceB VIP + XinZhi 2021 Year: www.deviceb.xyz/dev/subscriptions/

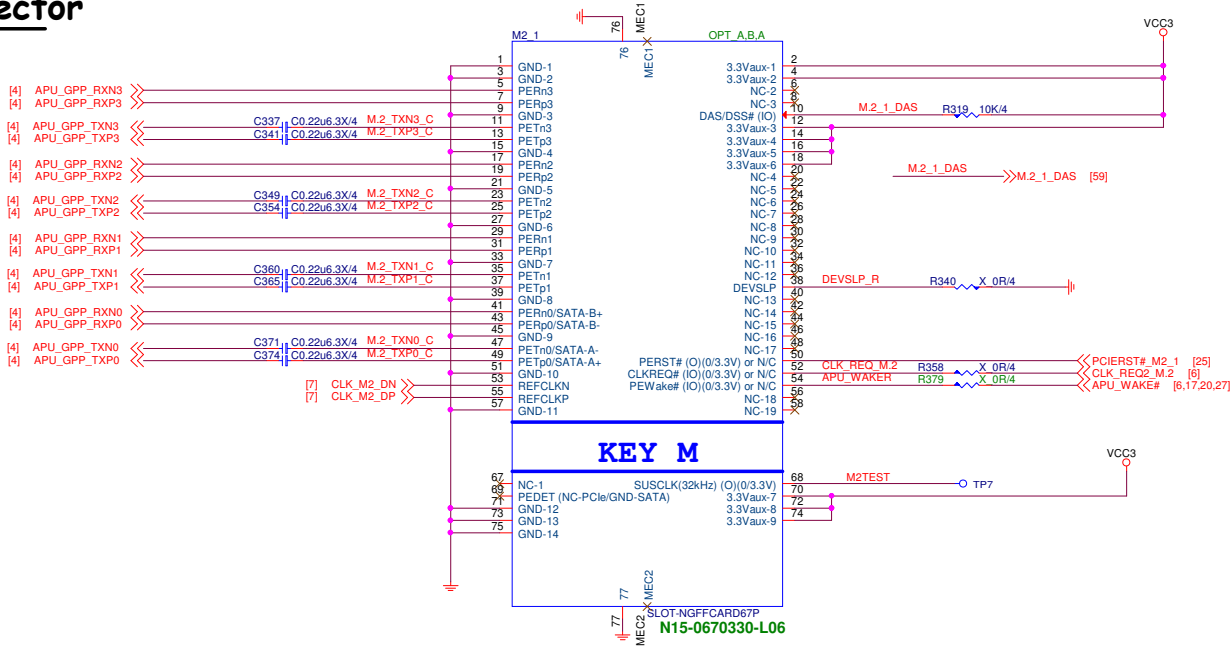
MICRO-START INTL CO.,LTD.

File: **SIO NCT6795D**

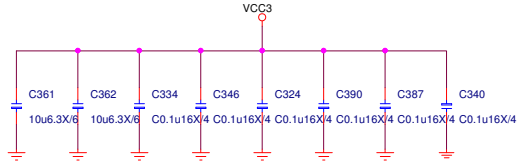
Size	Document Number	Rev
Custom	MS-7B79	1.1/2.1

Date: Tuesday, February 13, 2018 Sheet 24 of 72

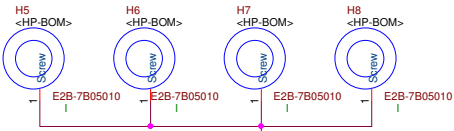
M.2_1 Connector
3.3V@2.5A



3.3V@2.5A



E2B-7984020-A89



Footprint: H_R240D173_BR189_PT

E2B-7B05010-A89

E2B-7B05010-A89

E2B-7B05010-A89

E2B-7B05010-A89

DeviceDB VIP + XinZhiZao 1 Year: www.device-db.xyz/dev/subscriptions/

Schematic Cfg		Project	
CFG-7B79-0A-X470-GAMING PRO		V	A
CFG-7B79-0A-X470-GAMING PLUS			

MSI Link to the Future MICRO-START INT'L CO.,LTD.			
Title M.2_1			
Size	Document Number	Rev	
Custom	MS-7B79	1.1/2.1	
Date:	Tuesday, February 13, 2018	Sheet	26 of 72

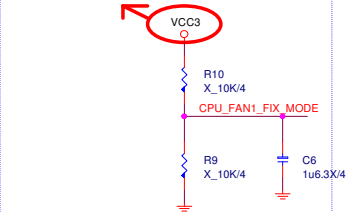
3.3V@2.5A

TYPE L : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

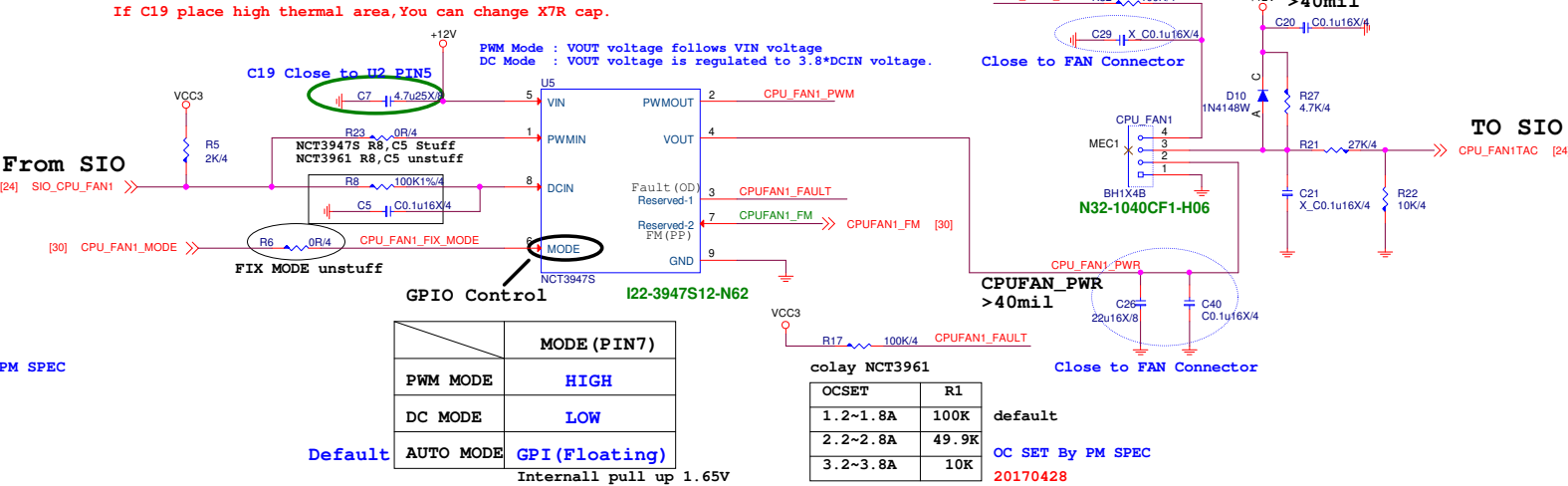
- 1.Mode GPIO BIOS can swtich PWM/DC MODE
- 2.FM:BIOS can read FAN PWM/DC MODE

CPU_FAN1

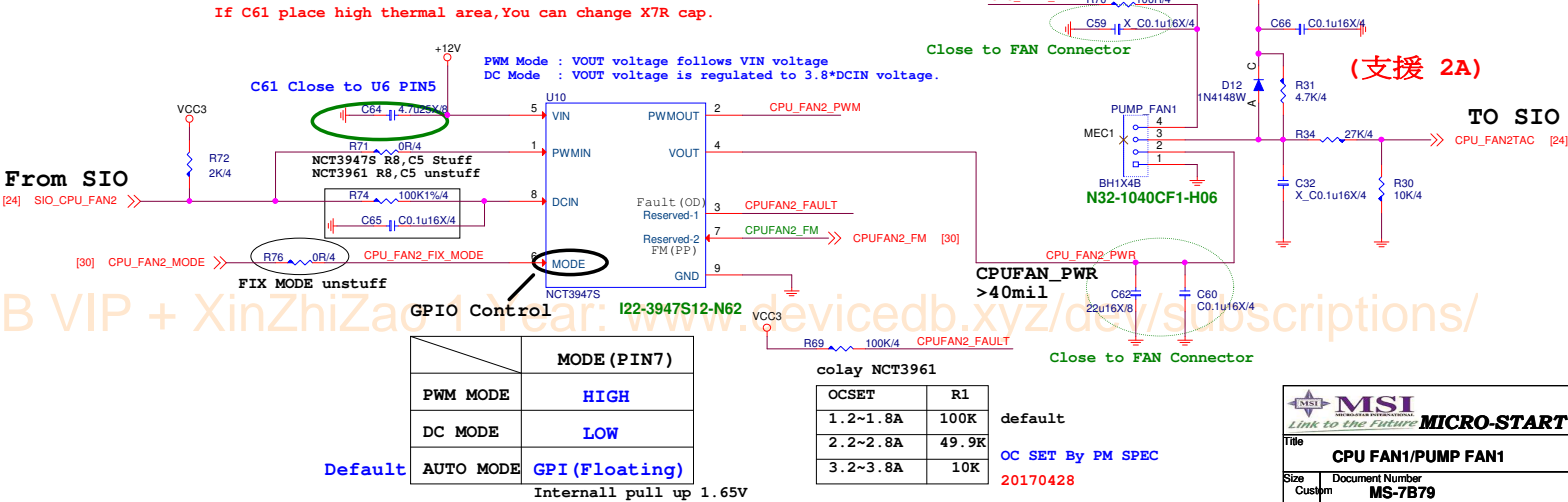
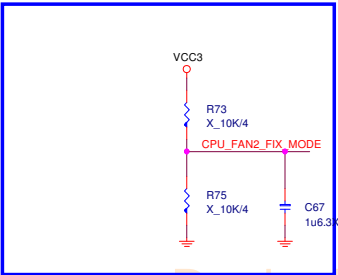
Avoid NCT3947S MODE PIN Leakage



Resever For FIX DC or PWM MODE USE By PM SPEC



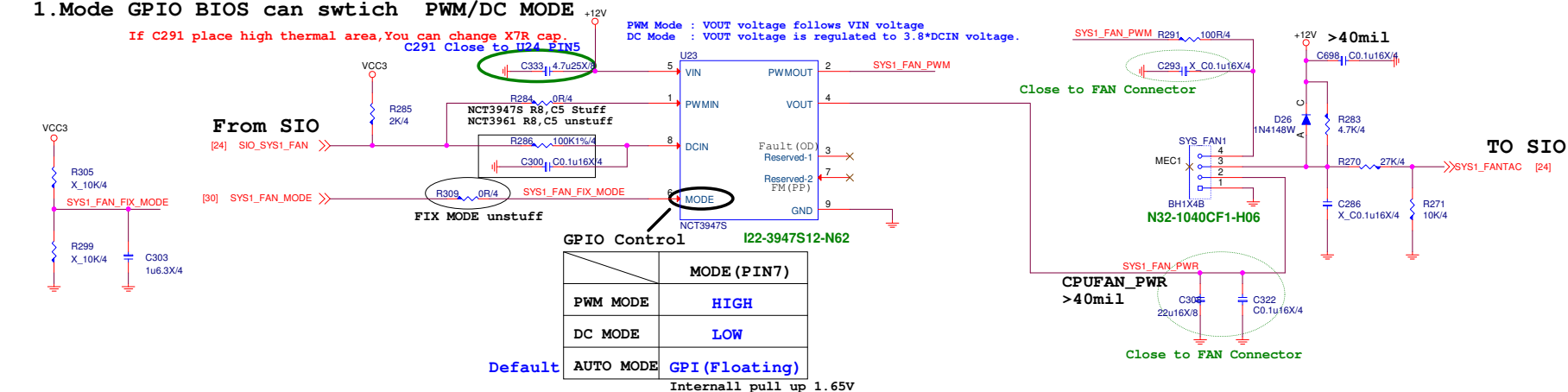
PUMP_FAN1



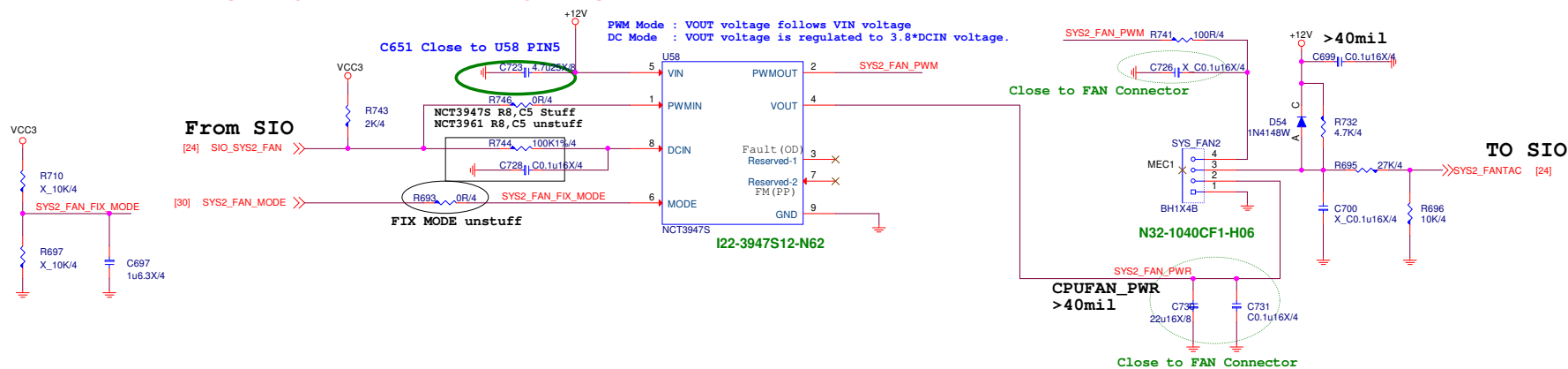
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

1.Mode GPIO BIOS can swtich PWM/DC MODE

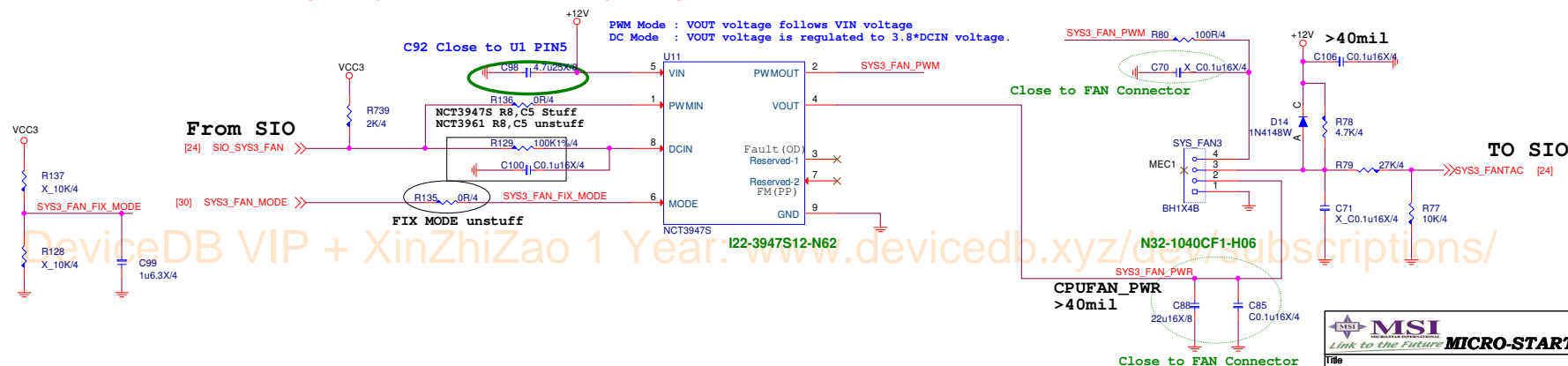
If C291 place high thermal area, You can change X7R cap.
C291 Close to U24 PIN5



If C651 place high thermal area, You can change X7R cap.

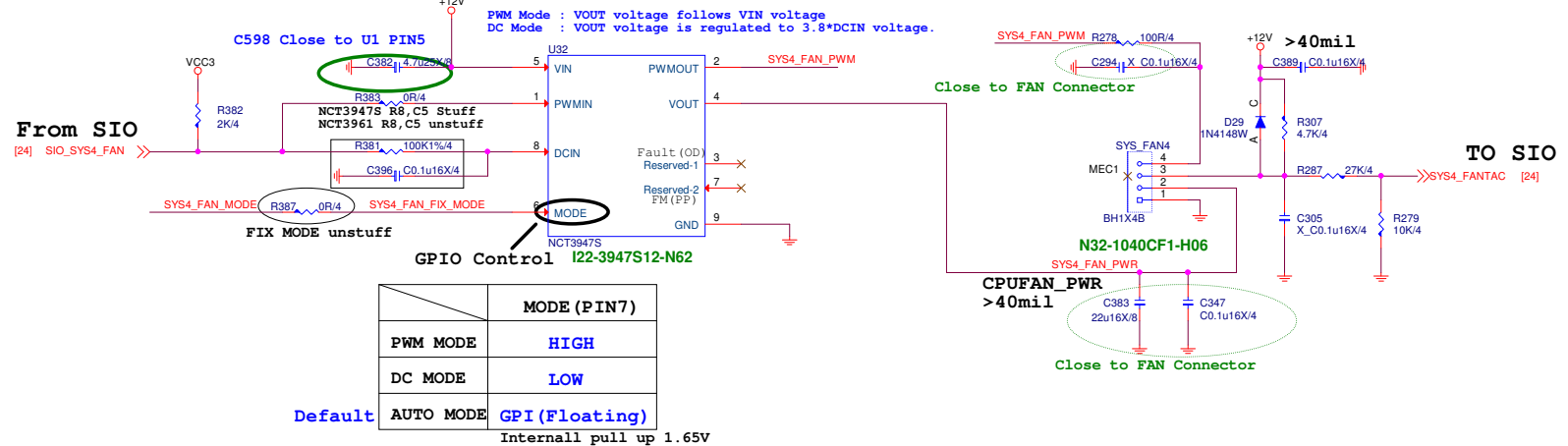
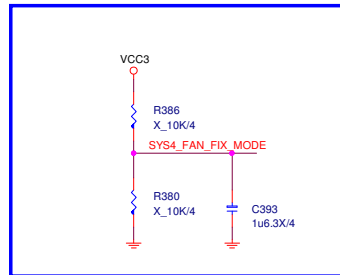


If C92 place high thermal area, You can change X7R cap.



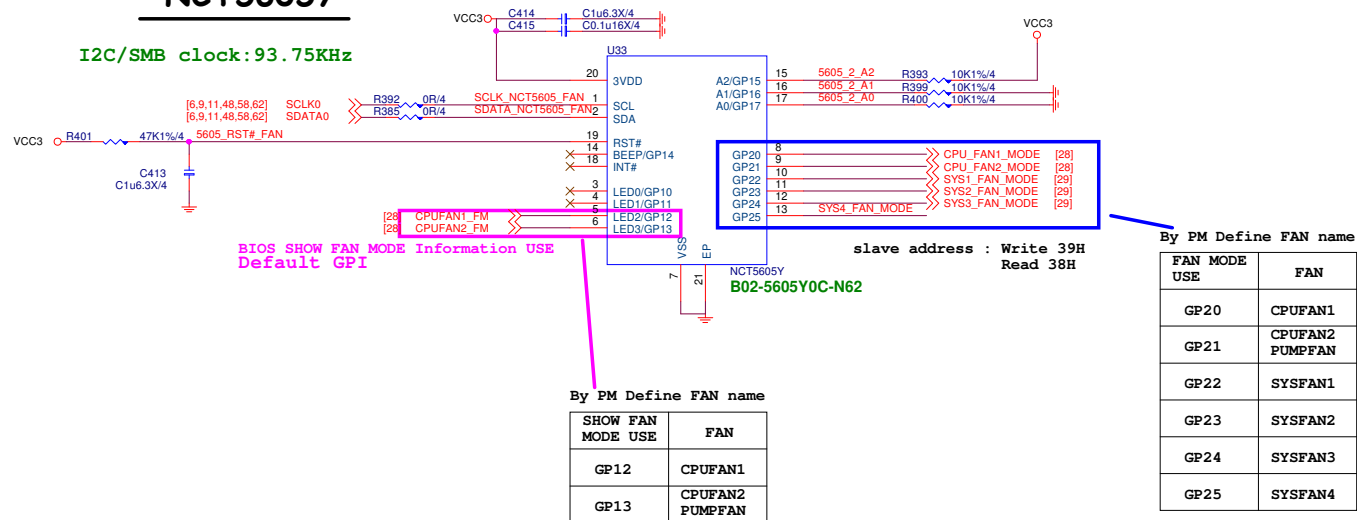
TYPE K : 4 PIN CPU FAN USE NCT3947S USE PCH GPIO CONTROL FAN MODE

If C598 place high thermal area, You can change X7R cap.



NCT5605Y

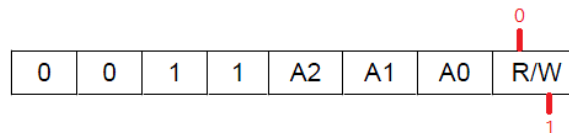
I2C/SMB clock:93.75KHz



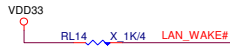
1. GENERAL DESCRIPTION

The NCT5605Y is a general purpose input/output IC with SMBus™ which provides 14 GPI/O pins. It also can provide SMBus™ address setting pins to set the address during power-on reset or from external reset.

NCT5605Y SMBus™ Address is:



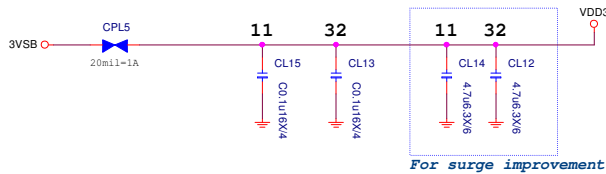
RTL8111H Giga LAN



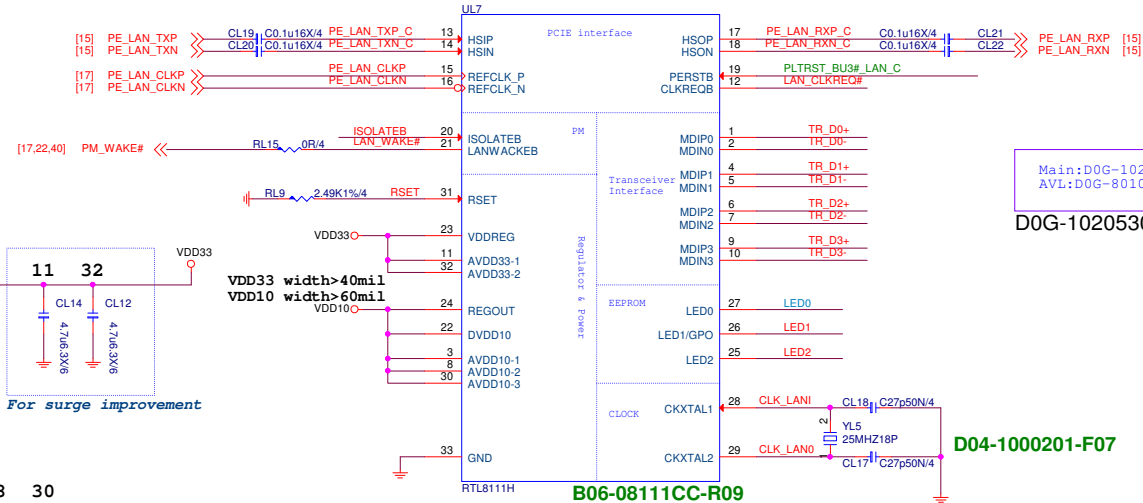
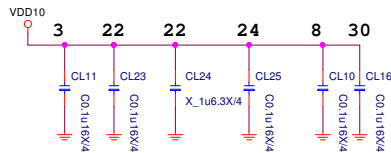
Remove pull-up R if R existence on motherboard
(or SB has internal pull-up R).



VDD33@65mA

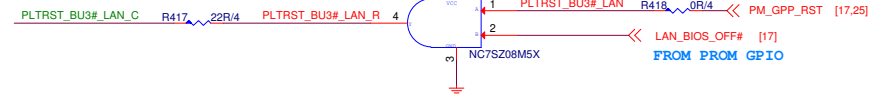
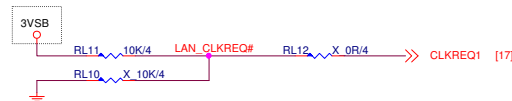


VDD10@150mA

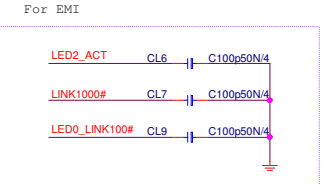
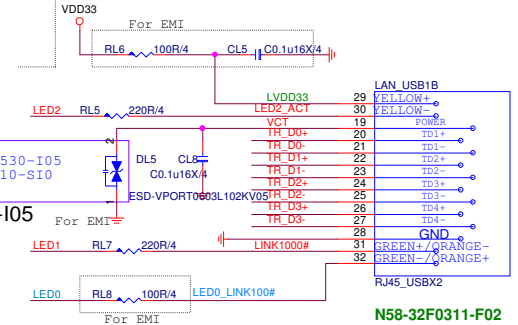


Pin33: 4 via from top layer to GND layer
and make the via at the center of IC.

Pull-up resistor RL9 required to either
3.3V suspend or core rail depending on
the power well of the PCH input CLKREQ# buffer.

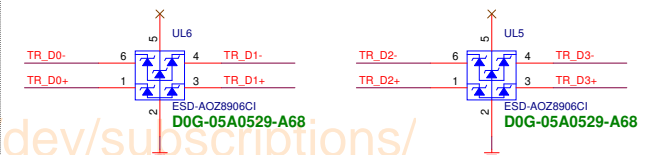


LAN Connector



ESD Protect close to connector

D0G-0200529-A68
D0G-0100619-I05



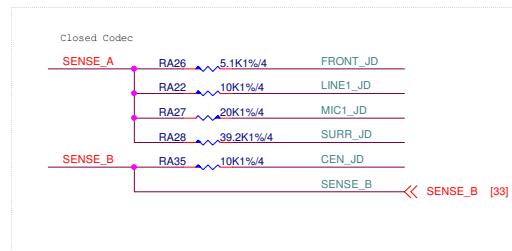
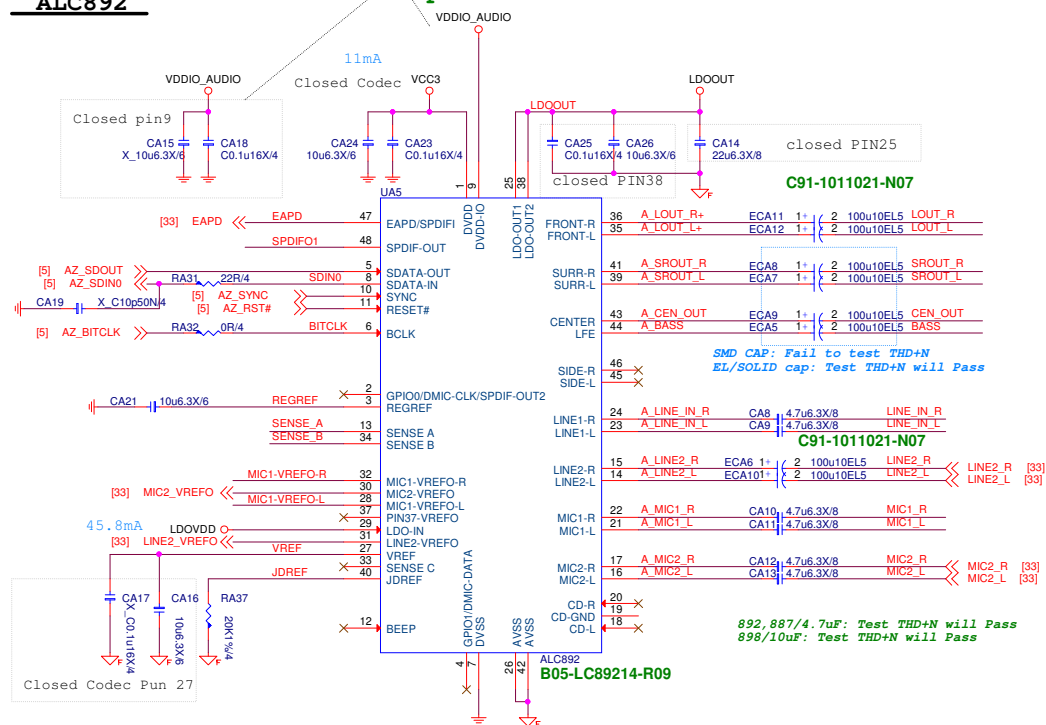
8111H POWER Consumption

	3.3V @ mA	mW
10 M Idle/TxRx	9.9/84.69	32.67/279.48
100 M Idle/TxRx	48.11/92.44	158.76/305.05
Giga Idle/TxRx	124.5/177.57	410.85/585.98
ALDPS	5.50	18.15

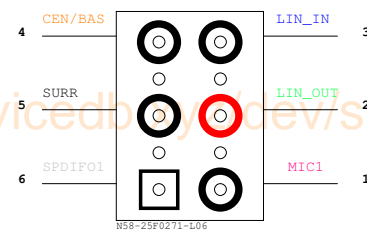
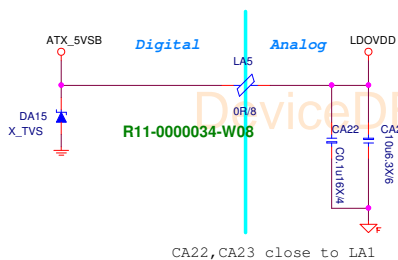
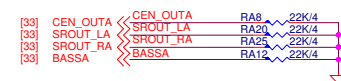
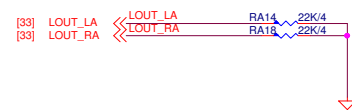
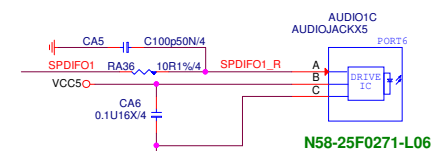
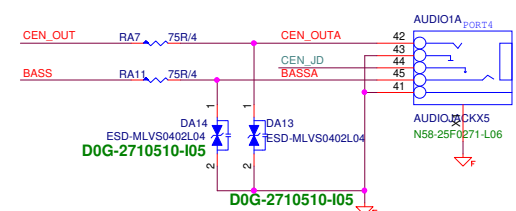
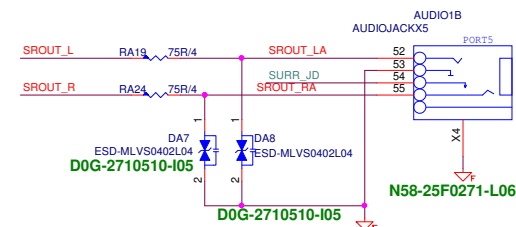
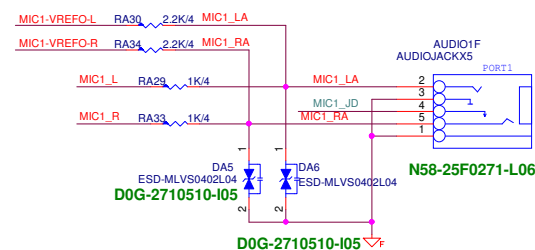
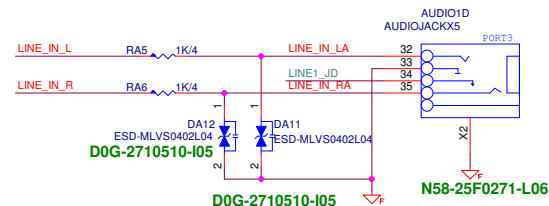
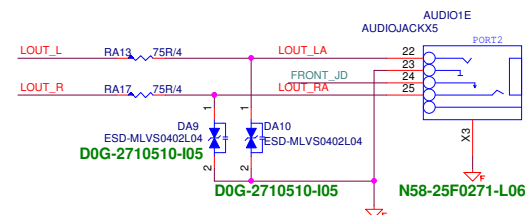
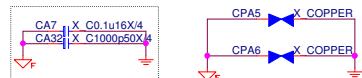
DeviceDB VIP + XinZhiZao 1 Year: www.device-db.xyz/dev/subscriptions/

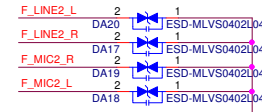
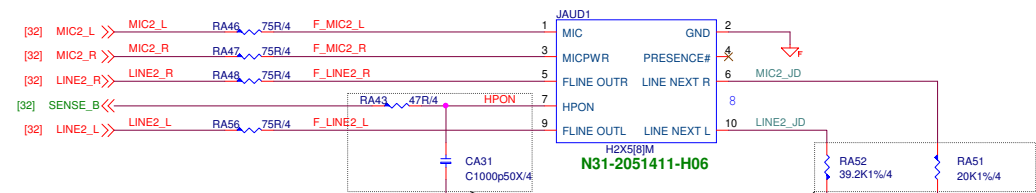
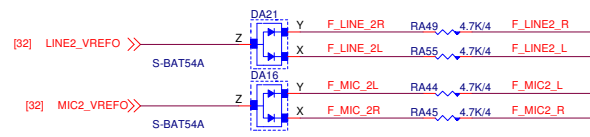
ALC892

Follow APU power well



EMI





D0G-2710510-I05

Close to Front panel

ESD protect

D0G-2710510-I05

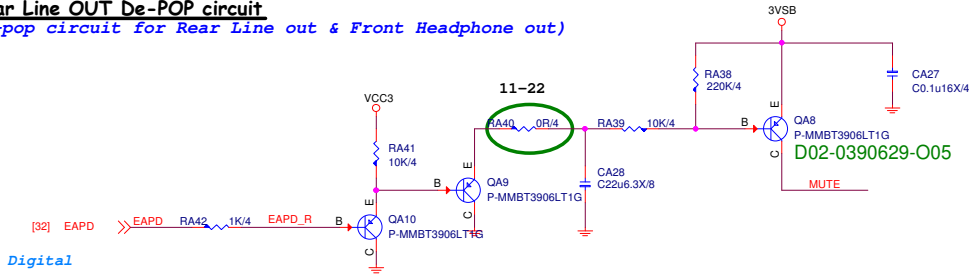
av1:D0G-2950500-SI0



Close to Front panel
For HDA/AC97 front cable.

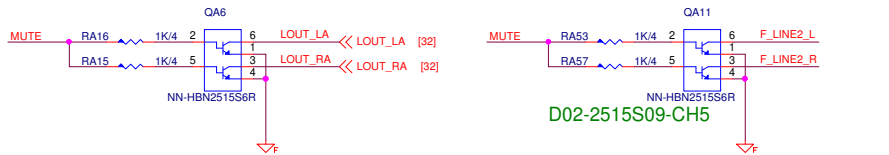
Rear Line OUT De-POP circuit

(De-pop circuit for Rear Line out & Front Headphone out)



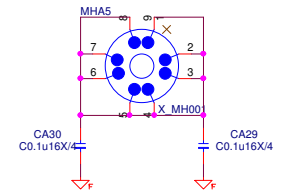
Digital

Analog



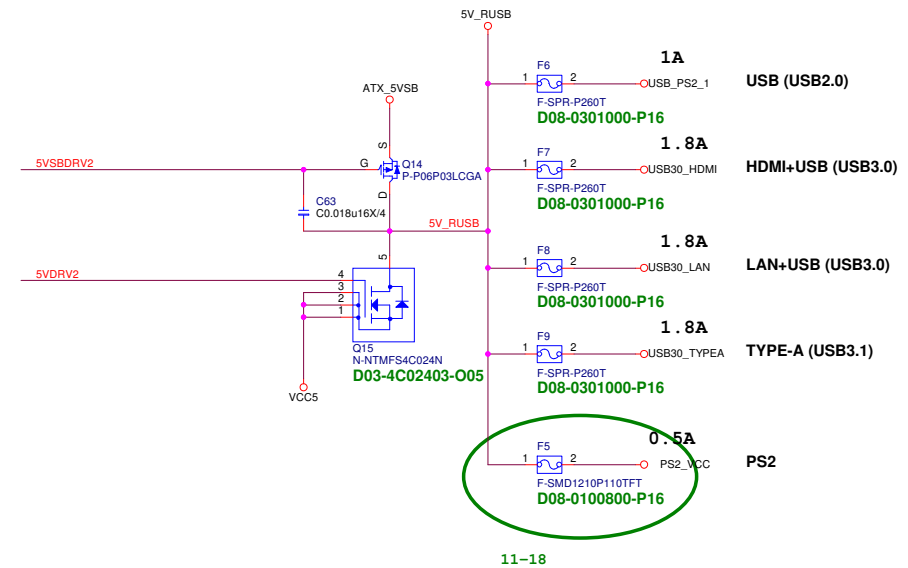
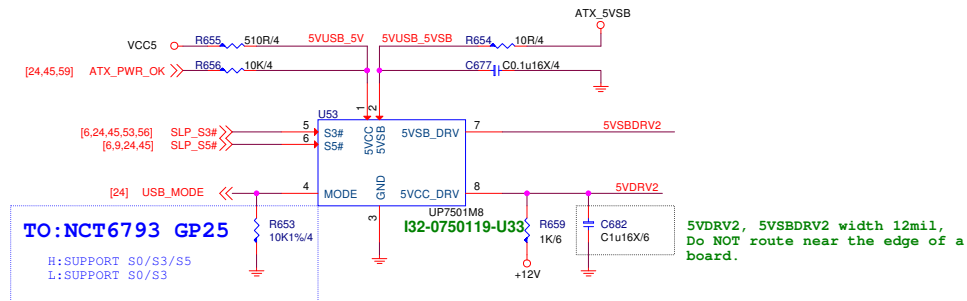
D02-2515S09-CH5

(add de-pop circuit by PM spec or customer request,
NOTE: add de-pop circuit need to change CA5, CA6, CA7, CA9, to TVS)



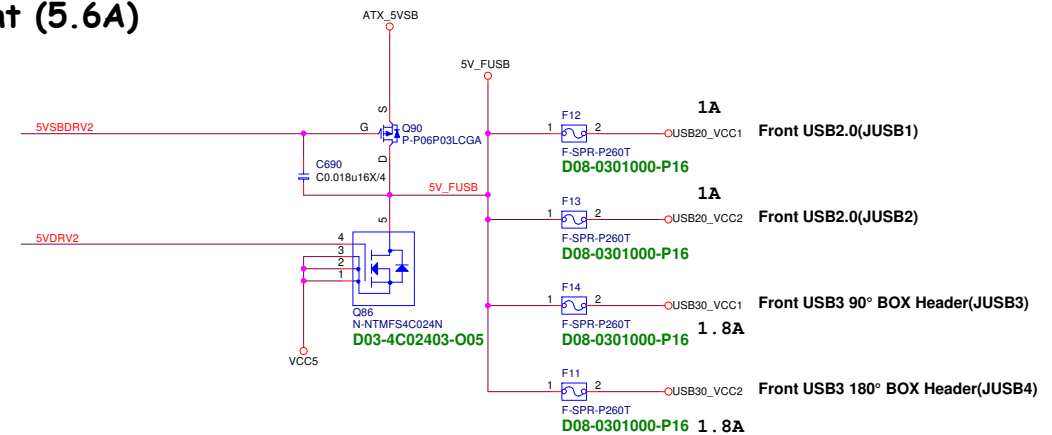
DeviceDB VIP + XinZhiZao 1 Year: www.device-db.xyz/dev/subscriptions/

USB Power

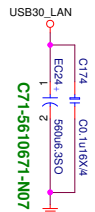
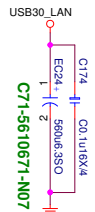


Rear (6.9A)

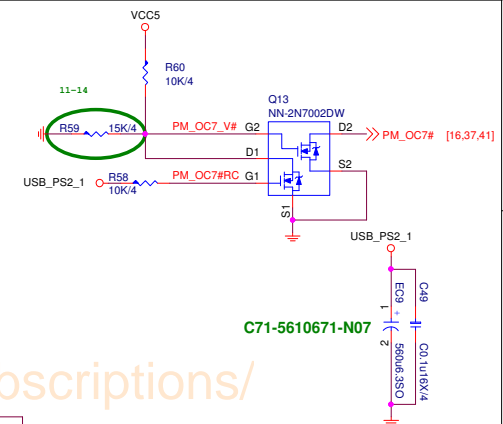
Front (5.6A)



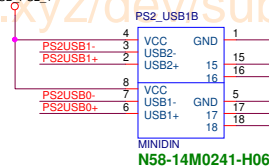
5V@1A



5V@1A



11-18 remove



USB30_HDMI

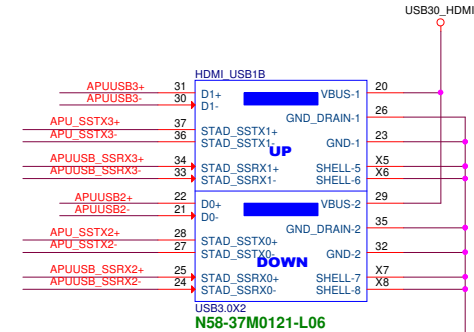
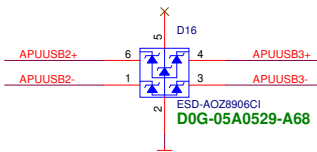
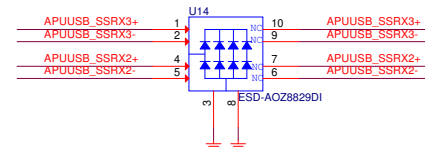
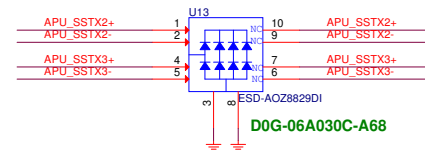
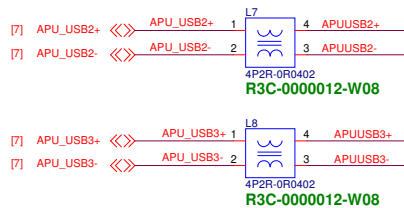
[7] APU_USB_SSTX2- <<> C108 C0.22u6.3X/4 APU_SSTX2-
[7] APU_USB_SSTX2+ <<> C107 C0.22u6.3X/4 APU_SSTX2+

[7] APU_USB_SSTX3- <<> C119 C0.22u6.3X/4 APU_SSTX3-
[7] APU_USB_SSTX3+ <<> C113 C0.22u6.3X/4 APU_SSTX3+

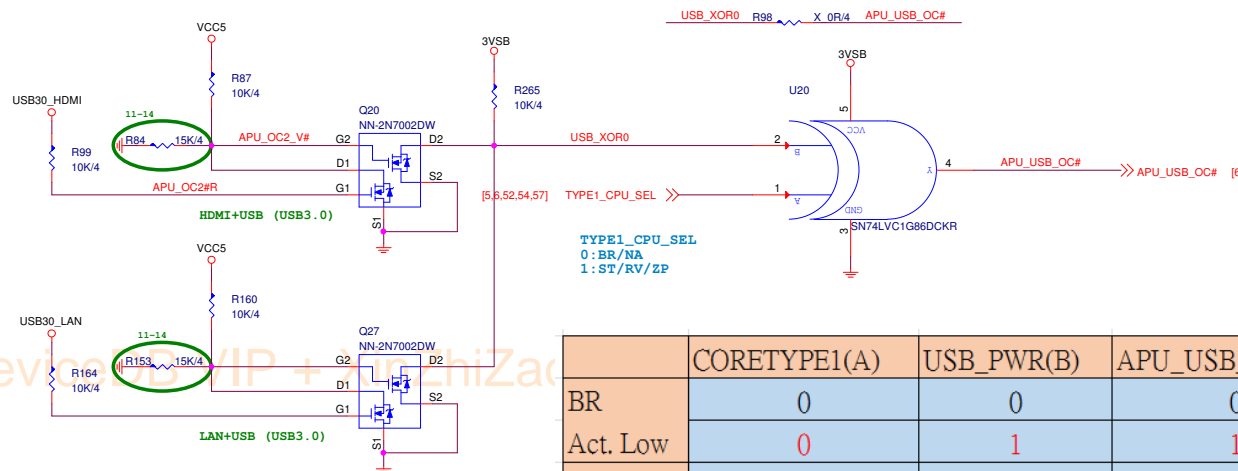
50726_1_12
Signals USB_SS_RX[0]P/N are connected to USB 3.1
connector through an XSR AC-coupling capacitor.

[7] APU_USB_SSRX2- <<> C133 C0.33u6.3X/4 APUUSB_SSRX2-
[7] APU_USB_SSRX2+ <<> C130 C0.33u6.3X/4 APUUSB_SSRX2+

[7] APU_USB_SSRX3- <<> C127 C0.33u6.3X/4 APUUSB_SSRX3-
[7] APU_USB_SSRX3+ <<> C125 C0.33u6.3X/4 APUUSB_SSRX3+



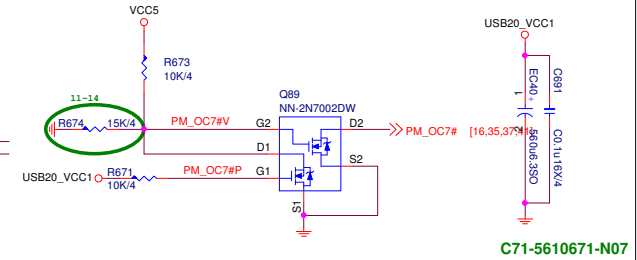
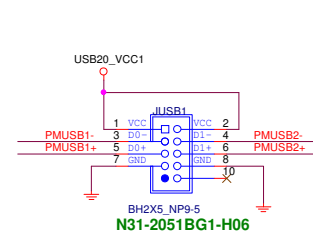
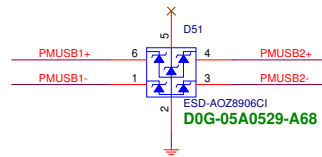
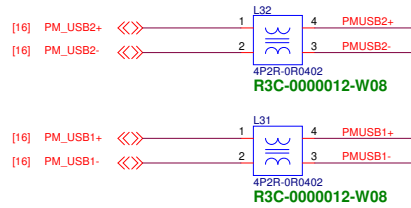
APU_USB_OC



	CORETYPE1(A)	USB_PWR(B)	APU_USB_OC(Y)
BR	0	0	0
Act. Low	0	1	1
SR	1	0	1
Act. High	1	1	0

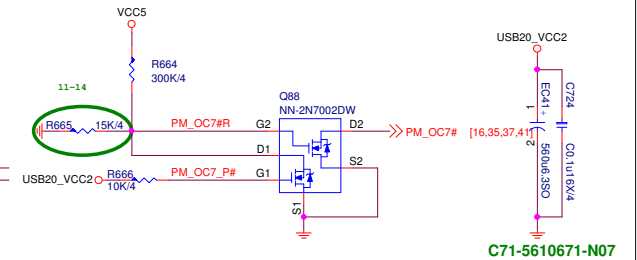
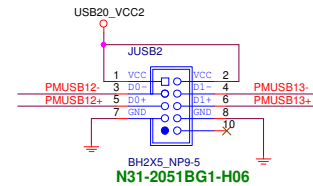
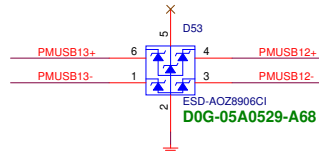
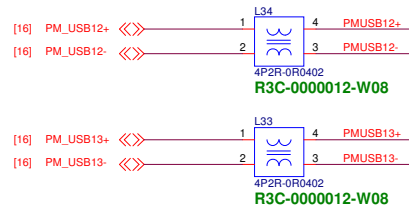
Front USB2.0 (JUSB1)

5V@1A



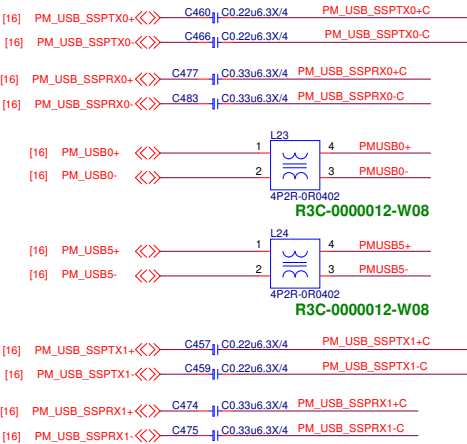
Front USB2.0 (JUSB2)

5V@1A

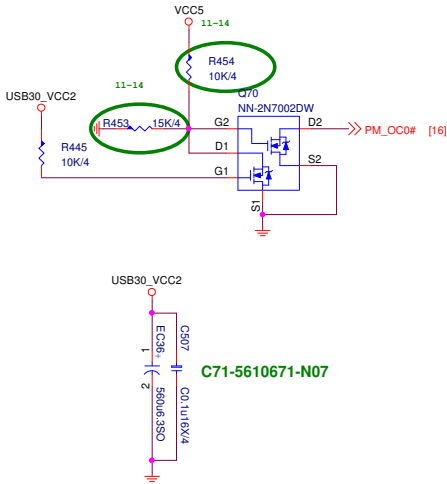
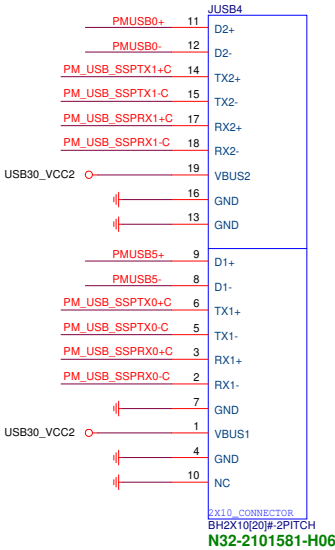
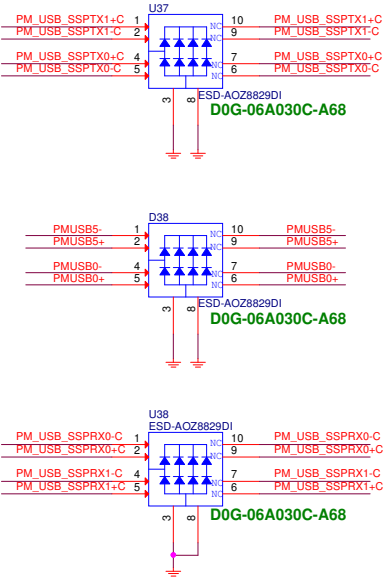


DeviceDB VIP + XinZhiZao 1 Year: www.device-db.xyz/dev/subscriptions/

Front USB3 90° BOX Header(JUSB4)
5V@1 . 8A

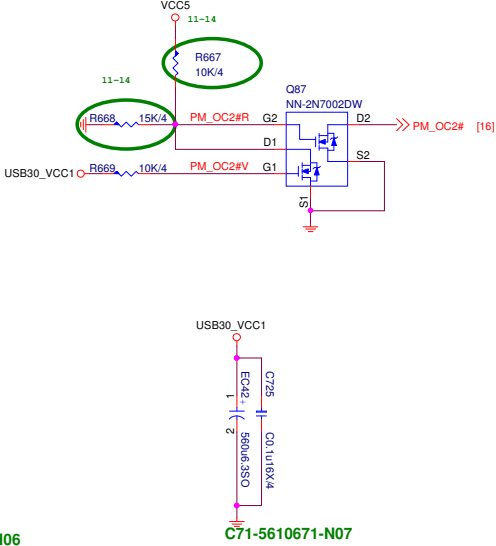
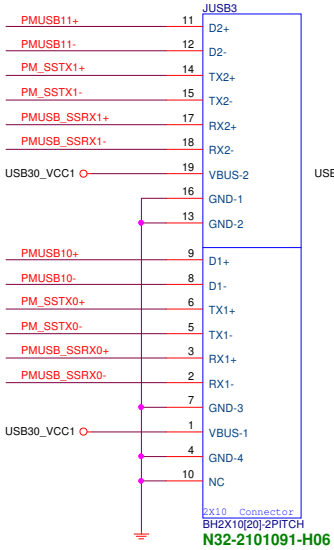
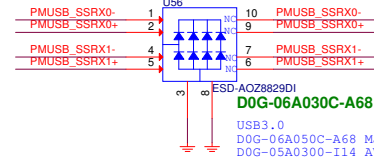
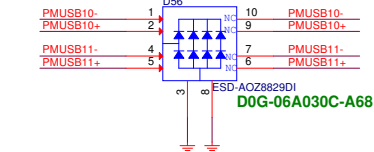
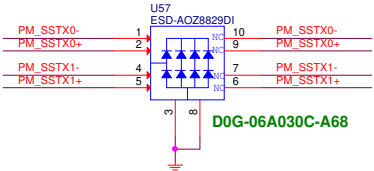
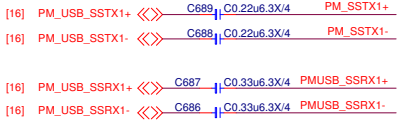
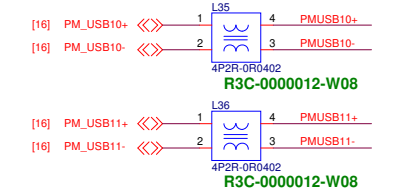
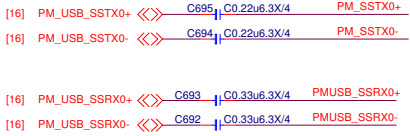


55551_1_07
Signals USB_SSP_RX[0]P/N are connected to USB 3.1 connector through an X5R or X7R AC-coupling capacitor 0.33uF 0402



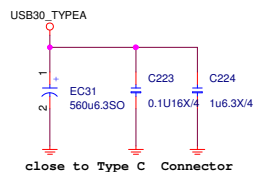
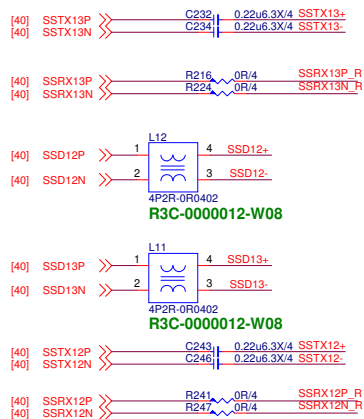
DeviceDB VIP + XinZhiZao 1 Year: www.device-db.xyz/dev/subscriptions/

Front USB3 180° BOX Header(JUSB3)
5V@1.8A

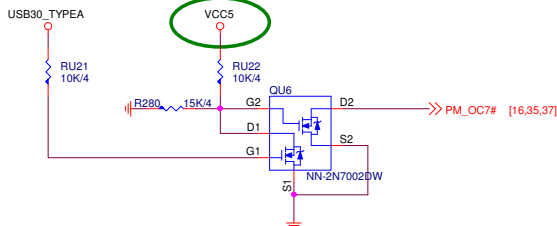
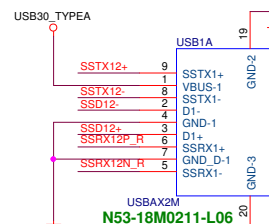
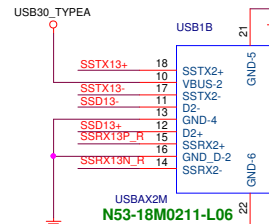
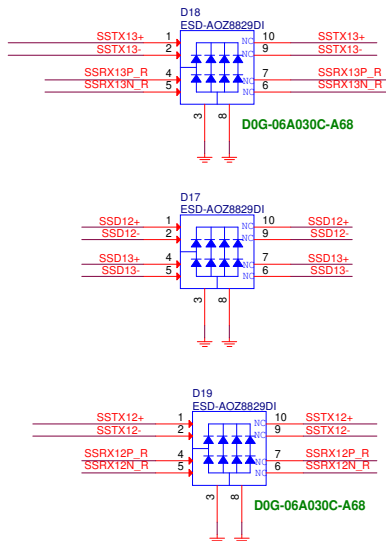


DeviceDB VIP + XinZhiZao 1 Year: www.device-db.xyz/dev/subscriptions/

Rear USB3.1 Type A

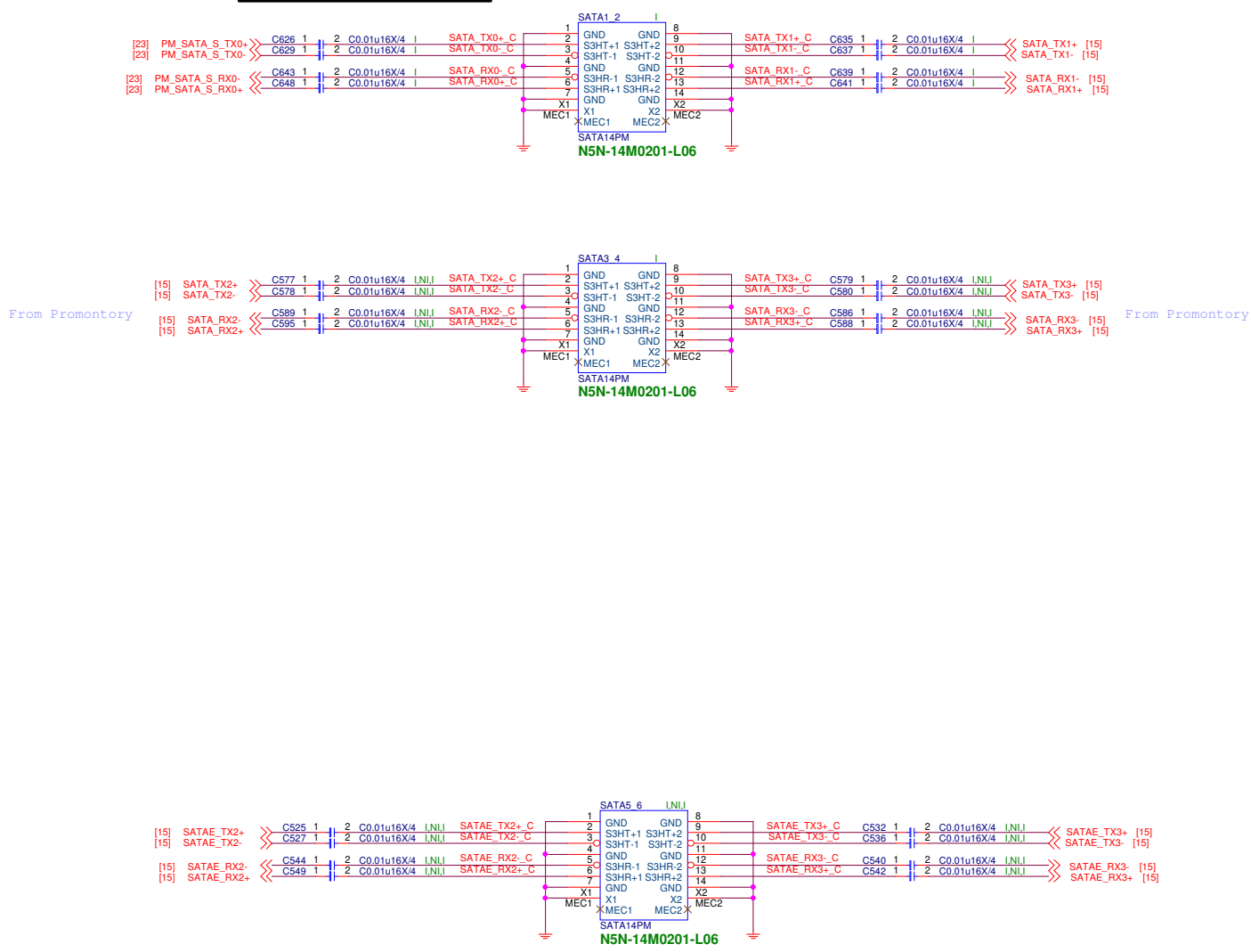


C71-5610671-N07




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SATA Connector



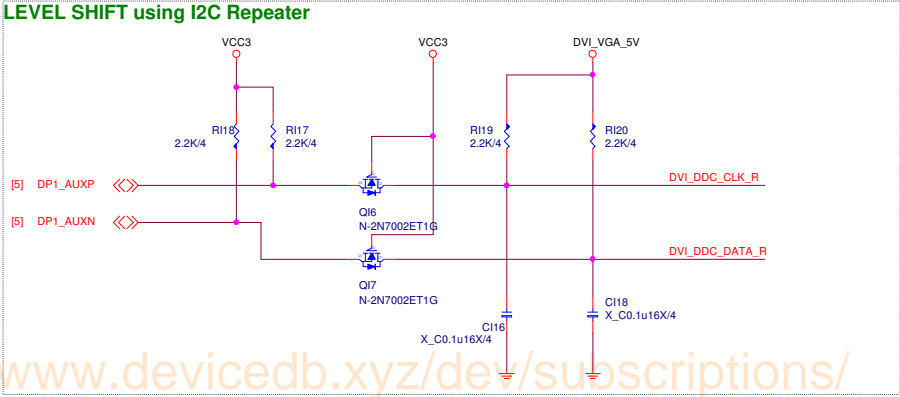
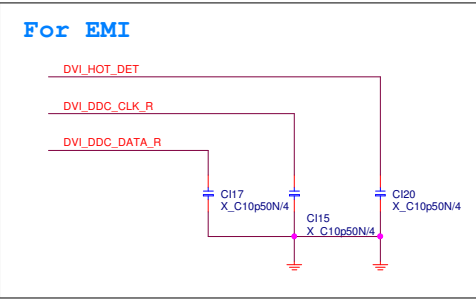
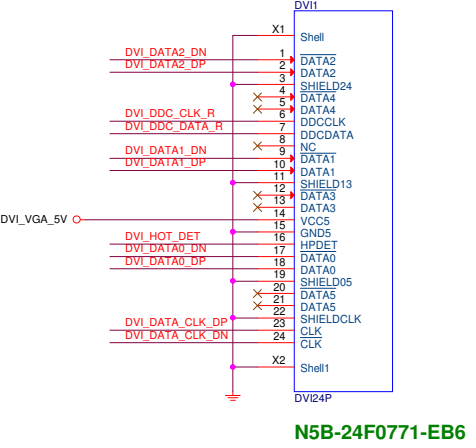
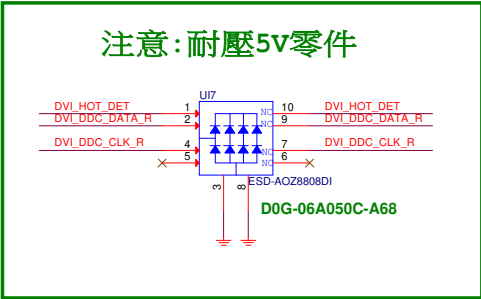
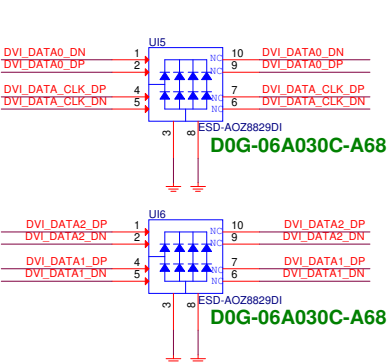
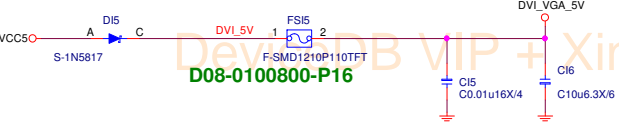
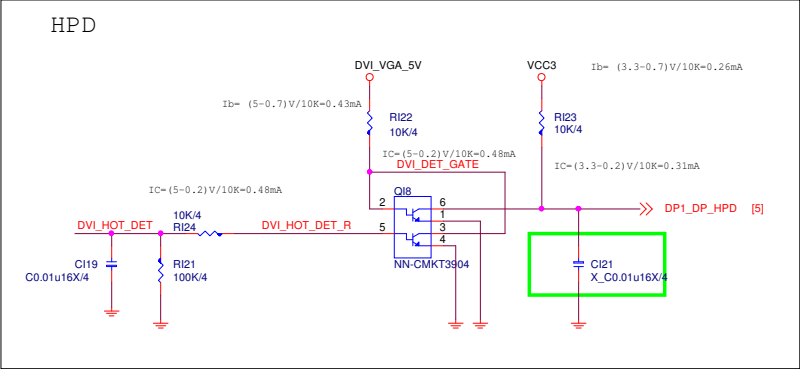
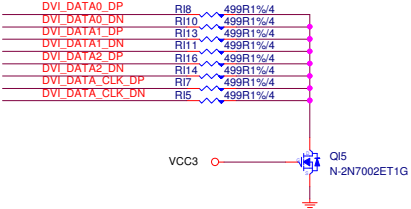
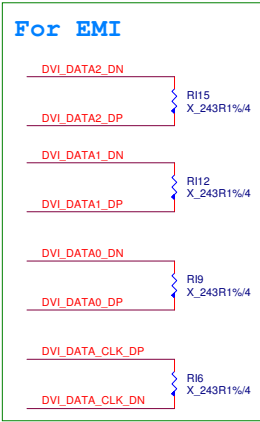
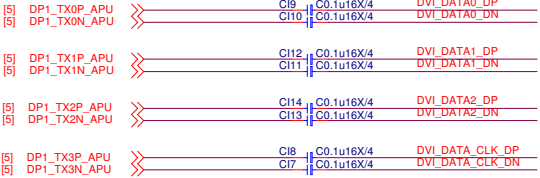
DeviceDB VIP + XinZhiZao 1 Year: www.device-db.xyz/dev/subscriptions/

Schematic Cfg		Project	
CFG-7B79-0A-X470-GAMING PRO		V	A
CFG-7B79-0A-X470-GAMING PLUS			

**MSI**
*Link to the Future***MICRO-START INT'L CO.,LTD.**

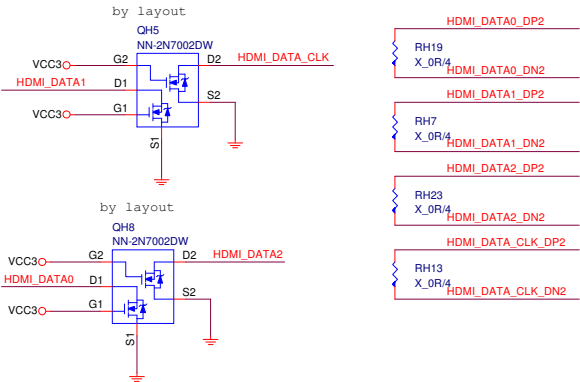
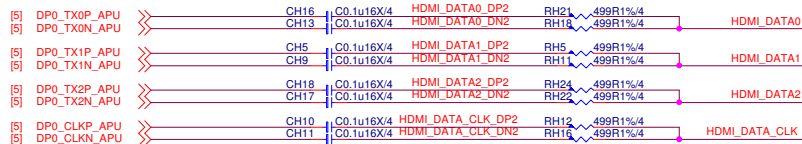
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Size	Custom	Document Number MS-7B79	Rev 1.1/2.1
Date:	Tuesday, February 13, 2018	Sheet	42 of 72

DVI CONNECTOR

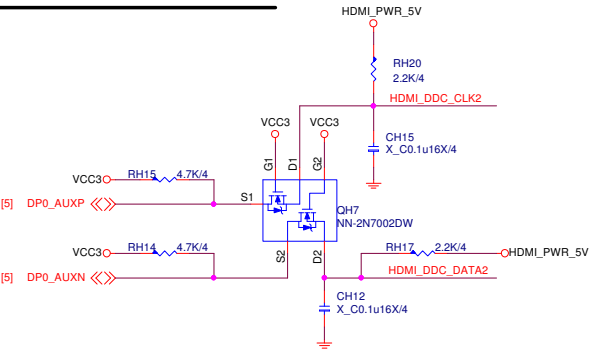


HDMI CONNECTOR

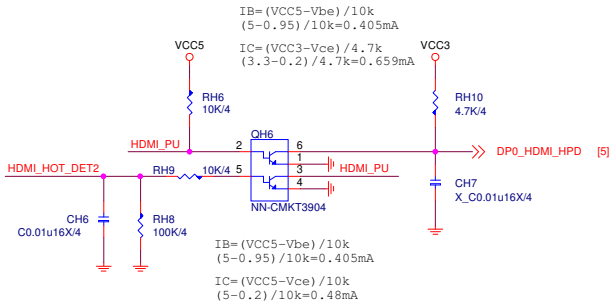
For HDMI 1.4



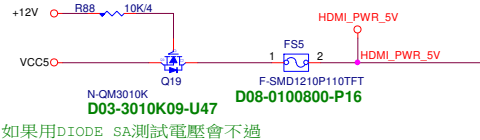
AUX Level Shifter



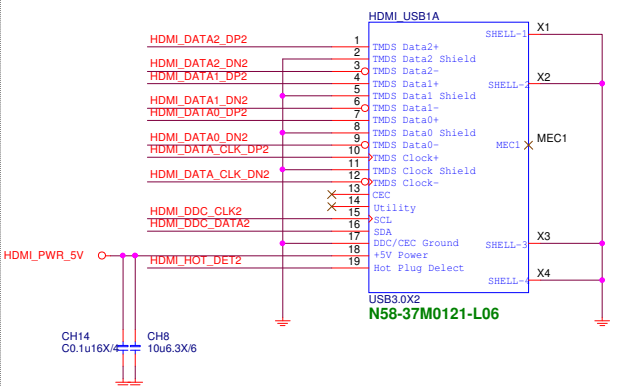
HPD Circuit



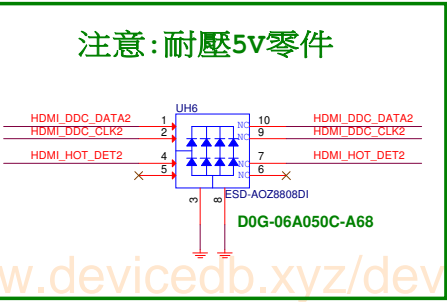
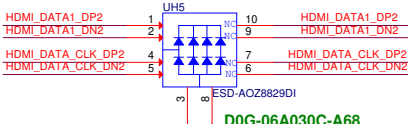
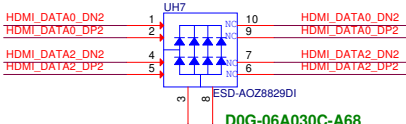
Connector Power



Connector



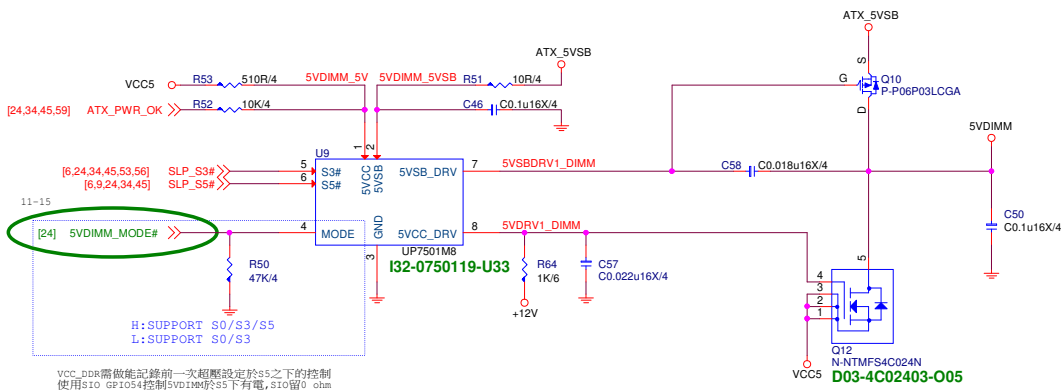
For EMI



注意:耐壓5V零件

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5VDIMM FOR DDR



3VSB cost down

3.3V@2.63A

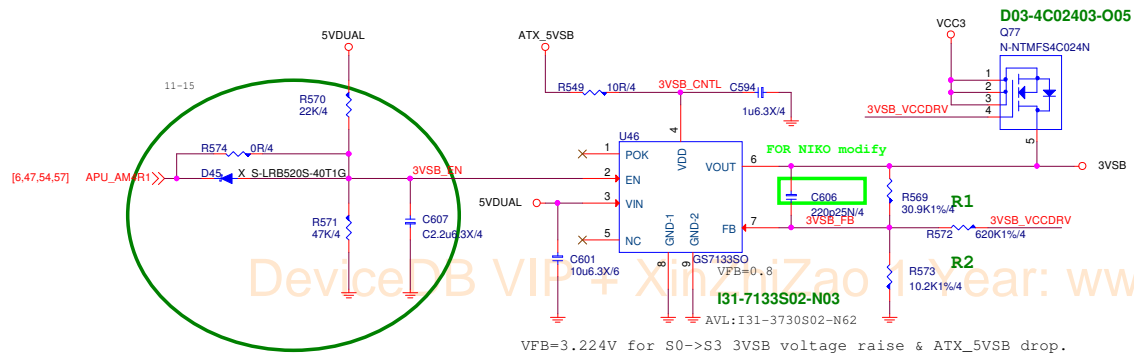
1.05V@0.05A

VDDBT_RTC_G@4.5uA

FCH@0.07A

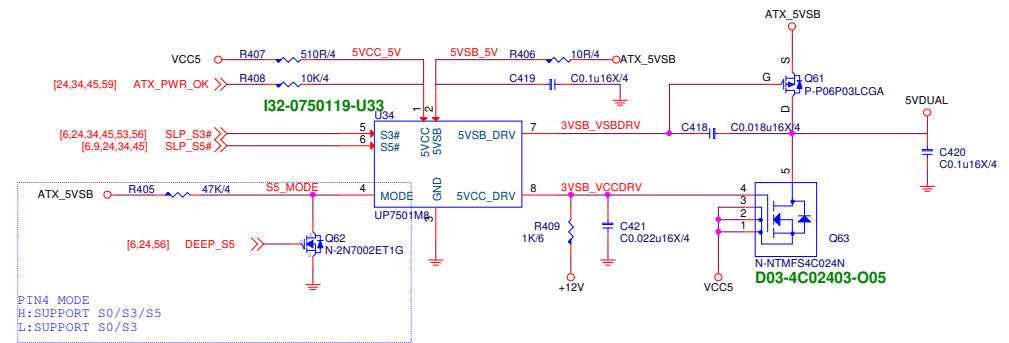
CPU@0.25A

PCIE*6 @2.25A

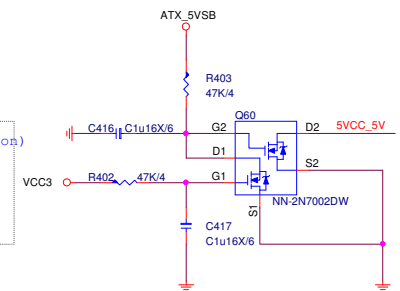


$$\begin{aligned} V_{out} &= V_{ref} * (1 + (R1/R2)) \\ &= 0.8 * (1 + (30.9K/10.2K)) \\ &= 3.22V \end{aligned}$$

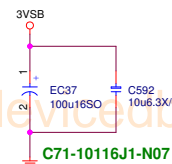
5VDUAL For 3VSB、CPU 1.8V、VDDP



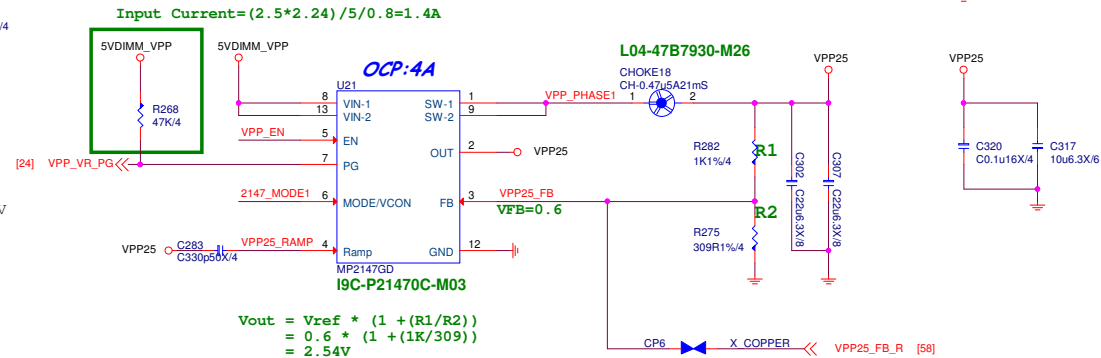
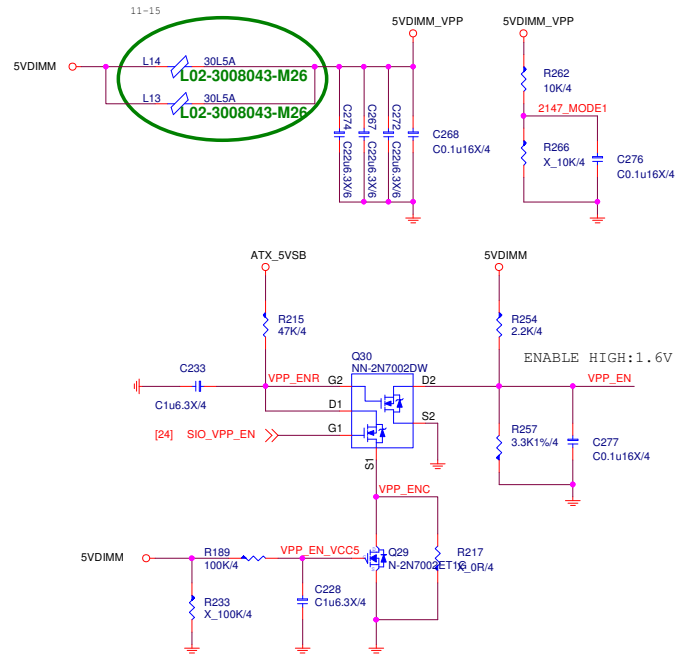
For power 700W solution (only for uP7501+uP7506 for 3VSB solution)
The power supply VCC3 delay 12ms after VCC5 assert.
The chip U7501 5VDRV1 work when the VCC5 ready
(When VCC5 up to 4.2V and the 5VDRV1 delay 6ms assert), but
VCC3 not ready and let the 3VSB sequence fail.



OCP=12A
2.63A

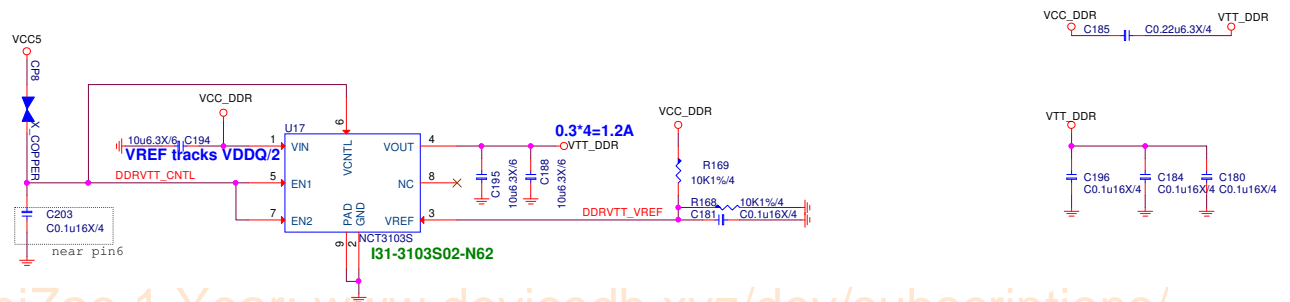


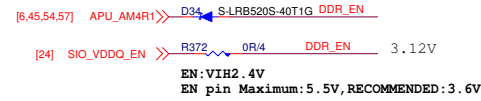
2.5V@2.24A



DDR VTT Power

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .

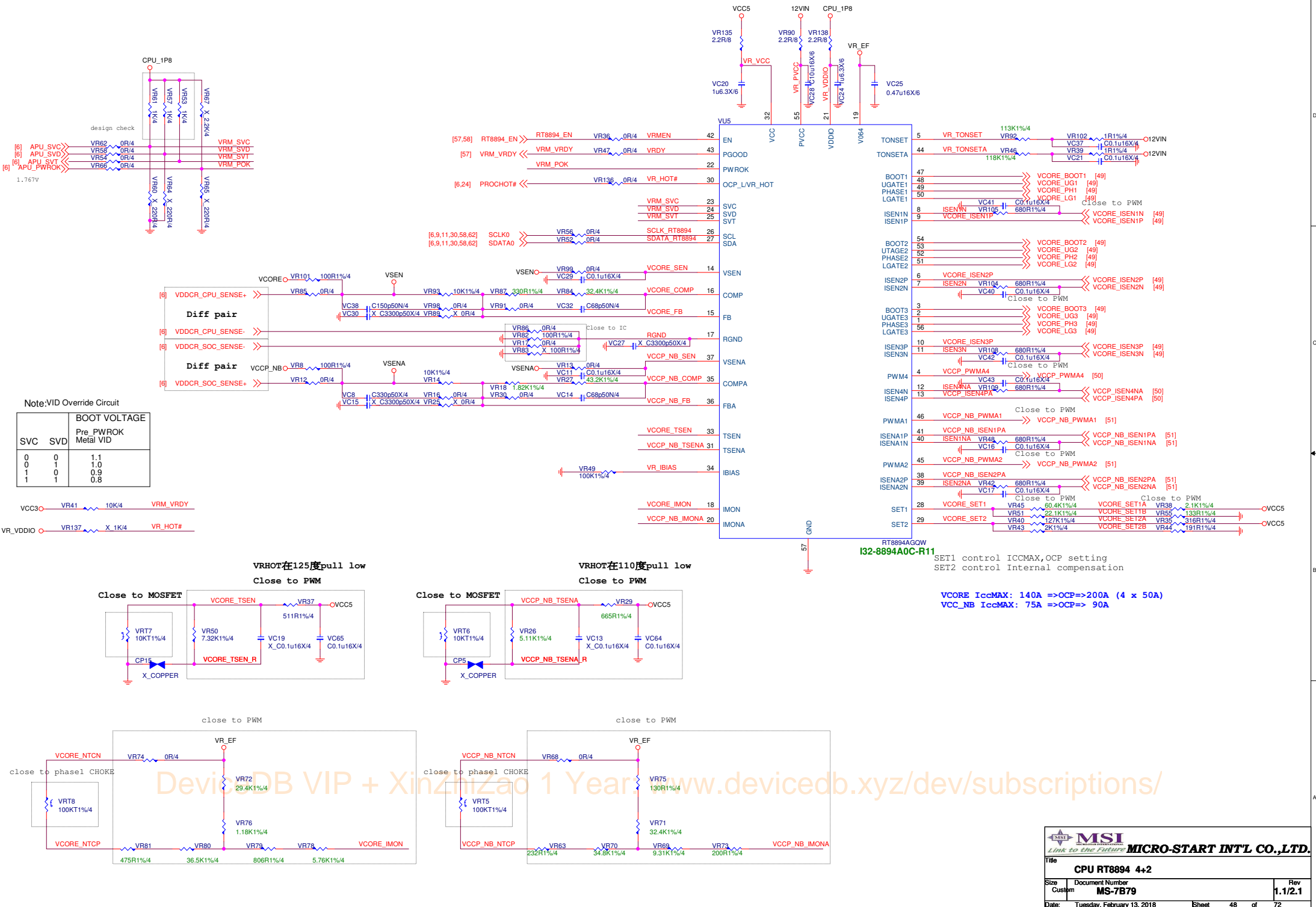


$$\begin{aligned} \text{Rocpset} &= 6.8\text{K} \\ \text{OCP} &= \text{Rocset} * 10\mu\text{A} / \text{Rdson (Low side)} \\ &= 6.8\text{K} * 10\mu\text{A} / 2\text{mohm} \\ &= 34\text{A} \end{aligned}$$


$$\begin{aligned} V_{out} &= V_{ref} * (1 + (R1/R2)) \\ &= 0.8 * (1 + (10K/19.1K)) \\ &= 1.218V \end{aligned}$$




C71-5610671-N07



Note:VID Override Circuit

SVC	SVD	BOOT VOLTAGE
		Pre_PWROK
		Metal VID
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

Vcore IccMAX: 140A =>OCP=>200A (4 x 50A)
VCC_NB IccMAX: 75A =>OCP=> 90A



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Title

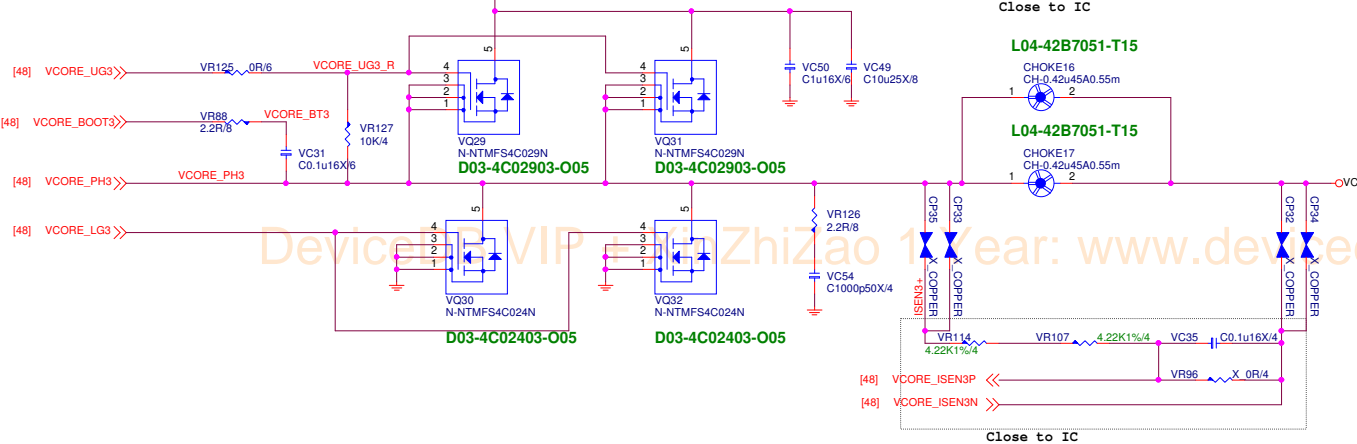
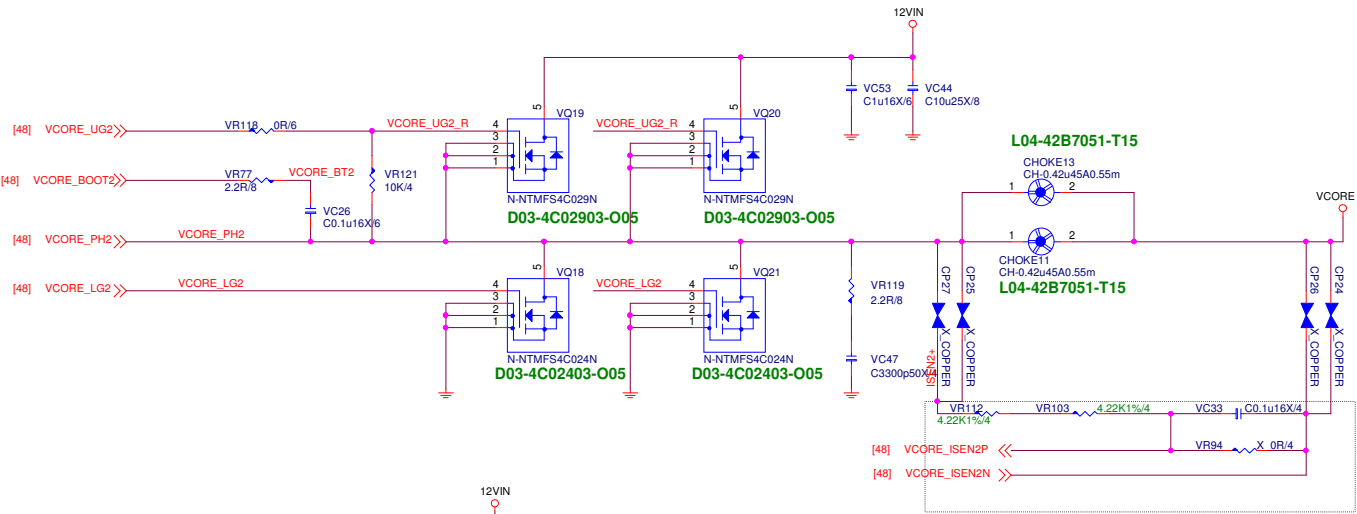
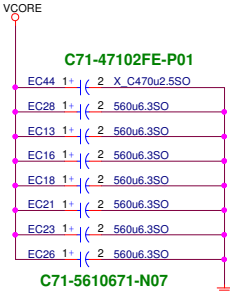
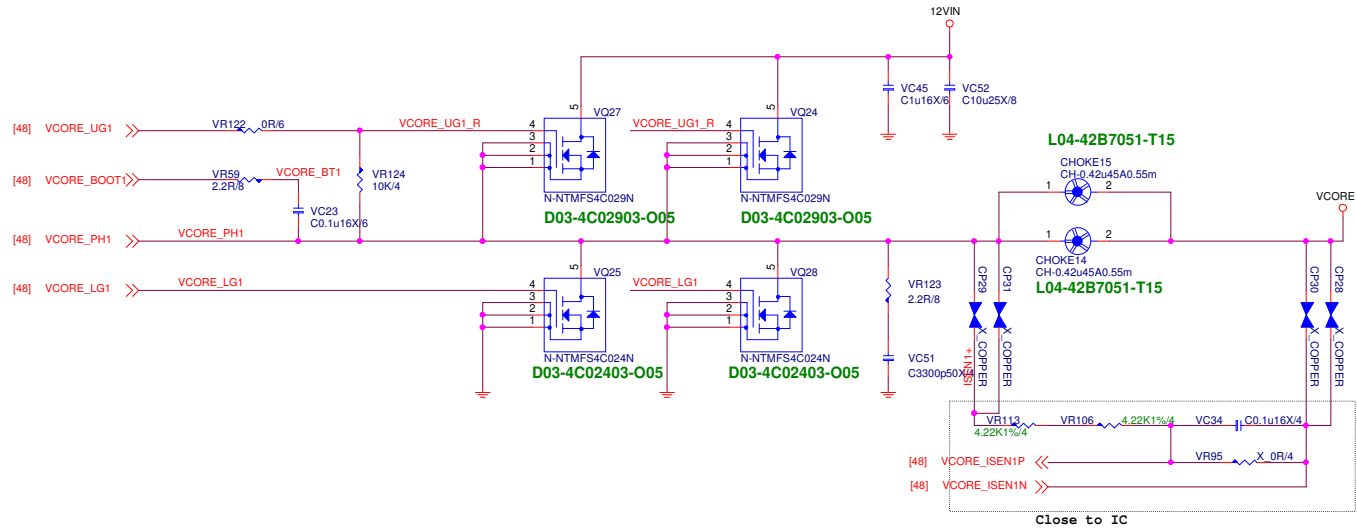
CPU RT8894 4+2

Size	Document Number	Rev
Custom	MS-7B79	1.1/2.1

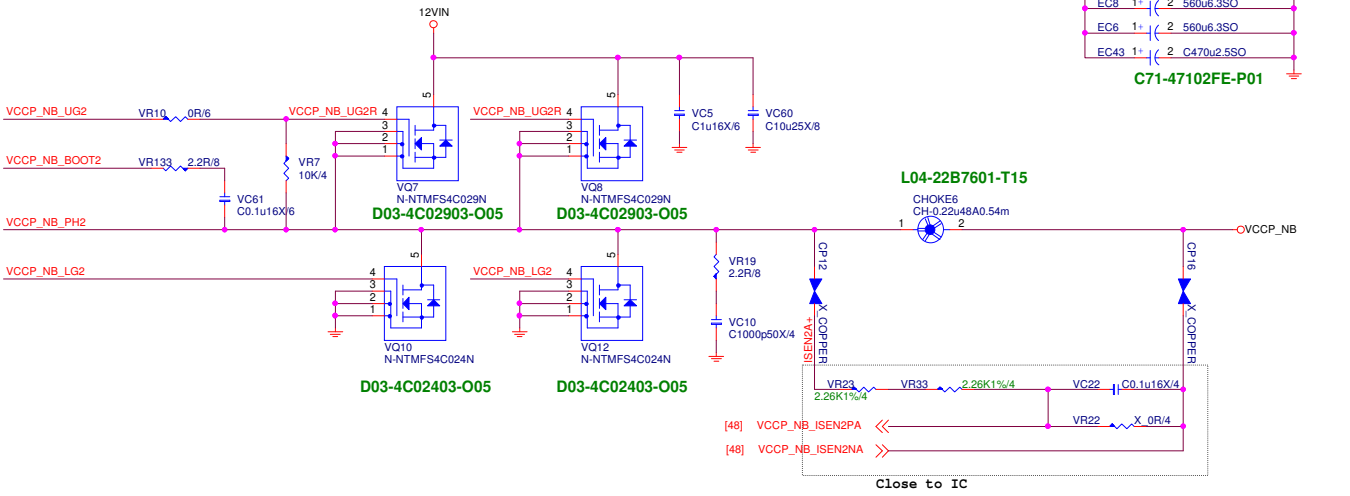
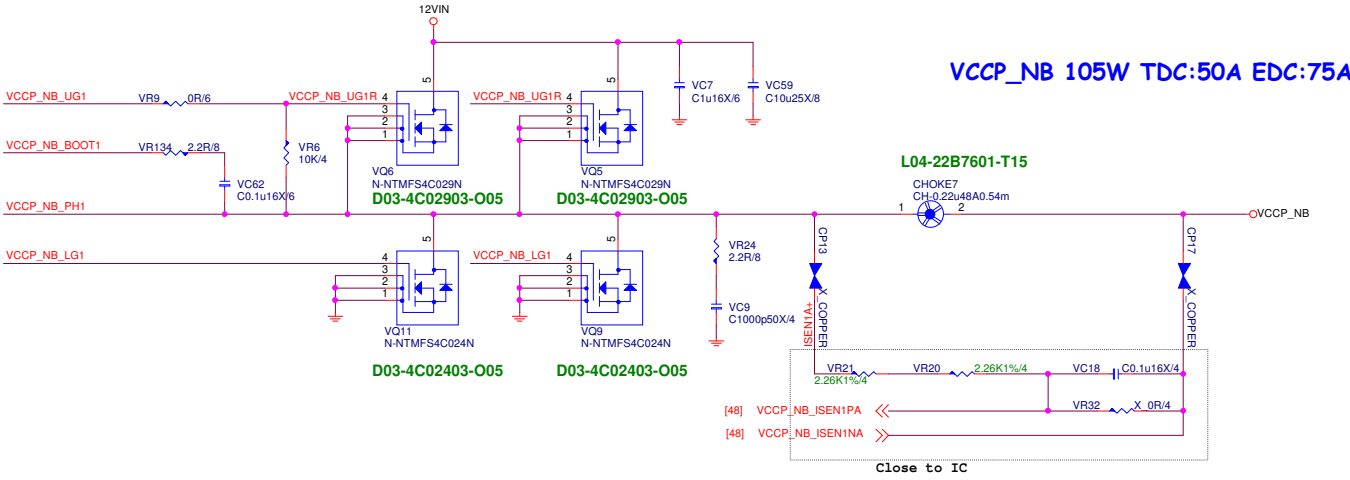
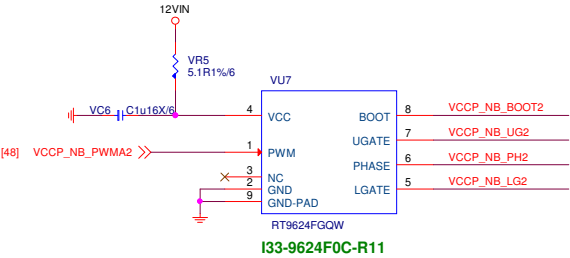
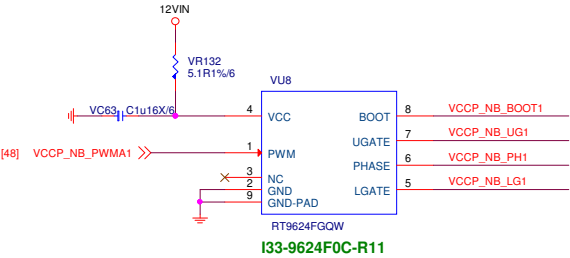
Date: Tuesday, February 13, 2018

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VCORE 105W TDC:95A EDC:140A



VCCP_NB 105W TDC:50A EDC:75A



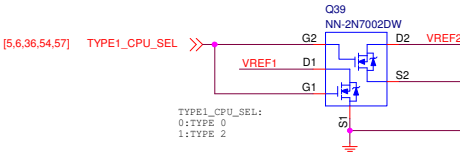
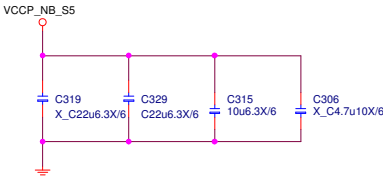
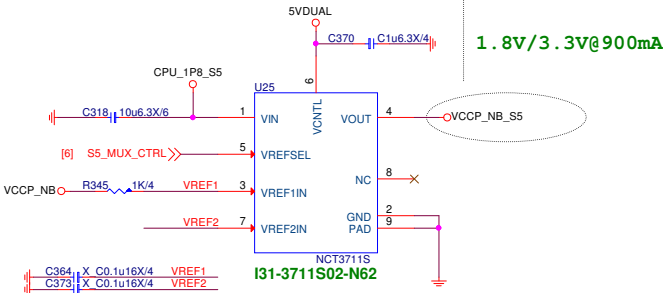
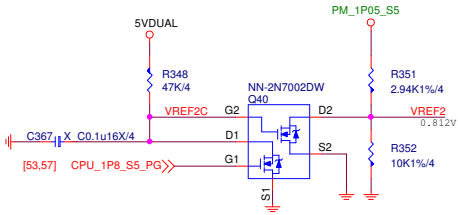
DeviceDB VIP + XinZhiZao 1 Year: www.device-db.xyz/dev/subscriptions/

FOR
VCCP_SOC_S5
0.9A

S5_MUX_CTRL
HIGH:S0
LOW: S3/S5

H: +VDDCR_FCH_ALW will track VDDNB
L: If VDDCR_SOC<0.775V (OR 0.85V),VDDCR_SOC_S5 =0.775V.
If VDDCR_SOC >= 0.775V (OR 0.85V) , VDDCR_SOC_S5 will track VDDCR_NB

(VDDCR_SOC_S5 is only used for AMD Family 15h Models 60h-6Fh processors)



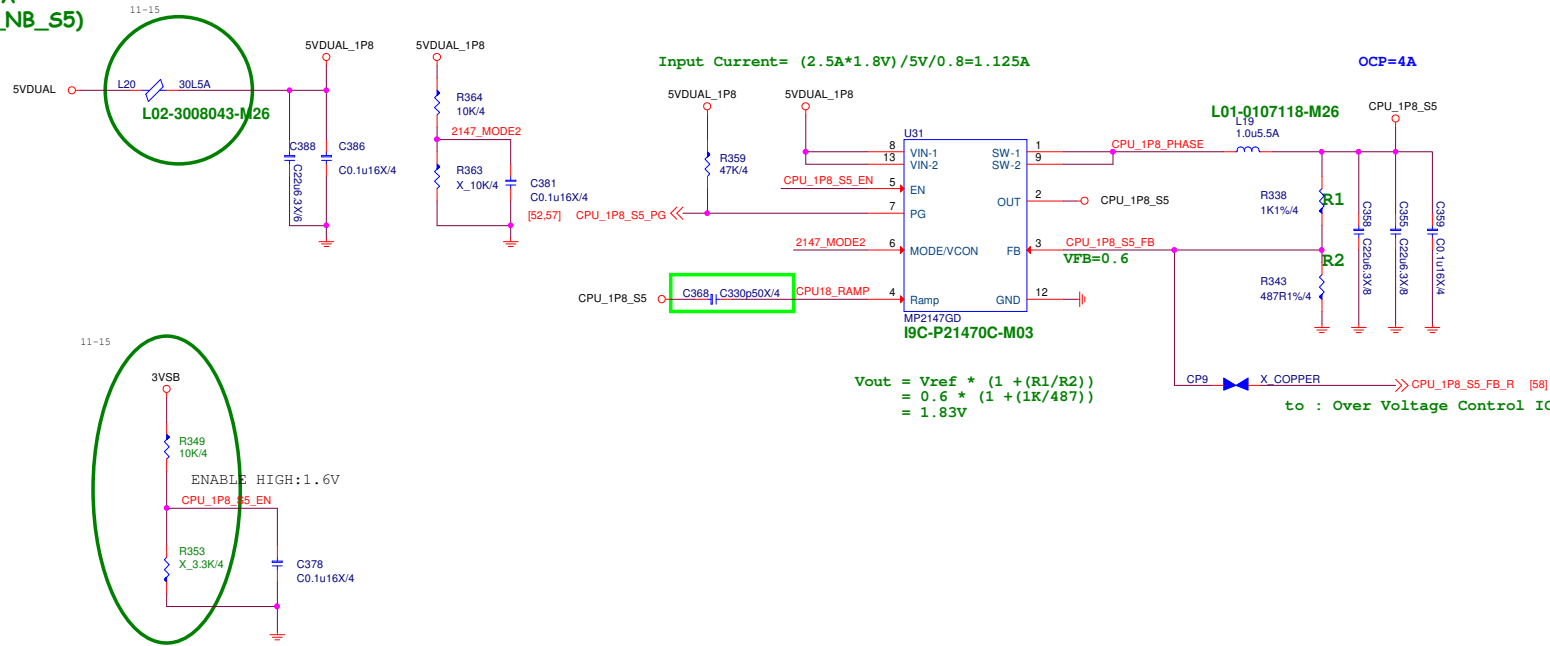
CPU	TYPE	TYPE1_CPU_SEL	TYPE0_CPU_SEL
BR	0	0	1
NA	2	0	0
SR	2	1	1
RV/ZP	3	1	0

CPU VCCP_NB_S5 ONLY SUPPORT TYPE0

DeviceDB VIP + XinZhiZao 1 Year: www.device-db.xyz/dev/subscriptions/

CPU 1.8V S5 @3.4A

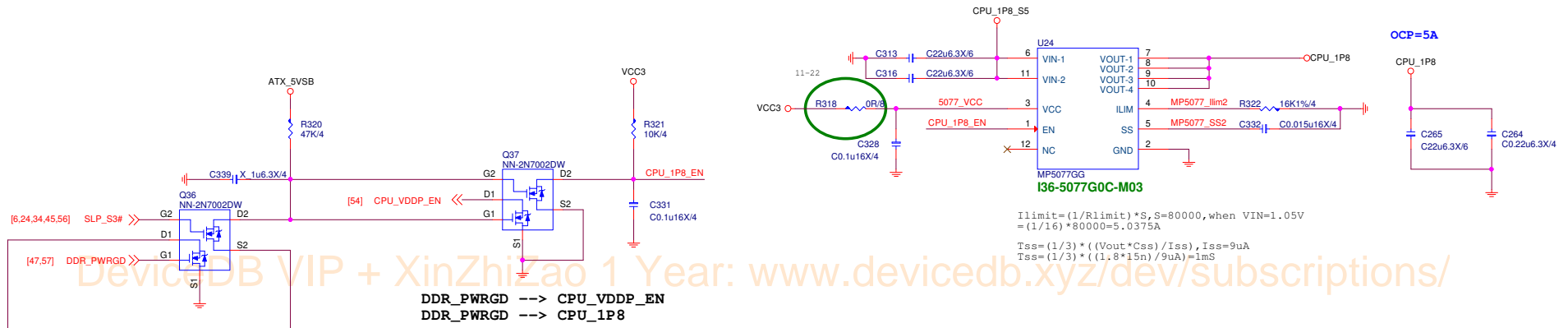
1.8V S5@0.5A
1.8V S0@2A
0.9A(VCCP_NB_S5)



CPU 1.8V S0

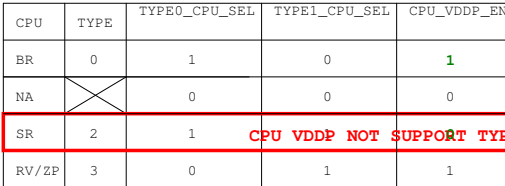
1.8V@2A

FOR VCCP_SOC@0.9A



Input Current= $(8.5A \cdot 1.05V) / 12V / 0.8 = 0.93A$

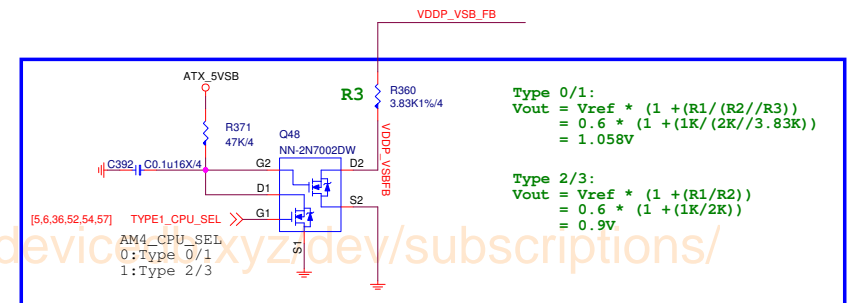
OCP=14A



(VDDCR_SOC_S5 is only used for AMD TYPE0)

Input Current=0.04A

default:0.775V,0.2A

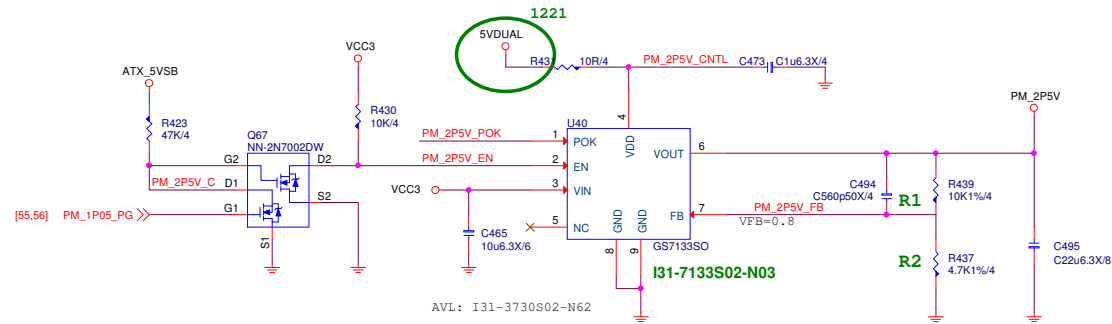


```
Type 0/1:
Vout = Vref * (1 + (R1/(R2//R3)))
      = 0.6 * (1 + (1K/(2K//3.83K)))
      = 1.058V
```

```
Type 2/3:
Vout = Vref * (1 + (R1/R2))
      = 0.6 * (1 + (1K/2K))
      = 0.9V
```

Promontory-2.5V

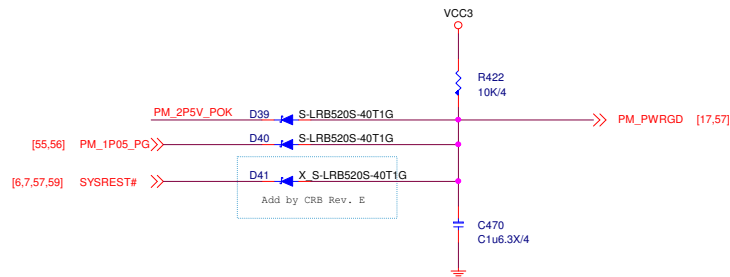
2.5V@900mA



$$V_{out} = V_{ref} * (1 + (R1/R2))$$

$$= 0.8 * (1 + (10K/4.7K))$$

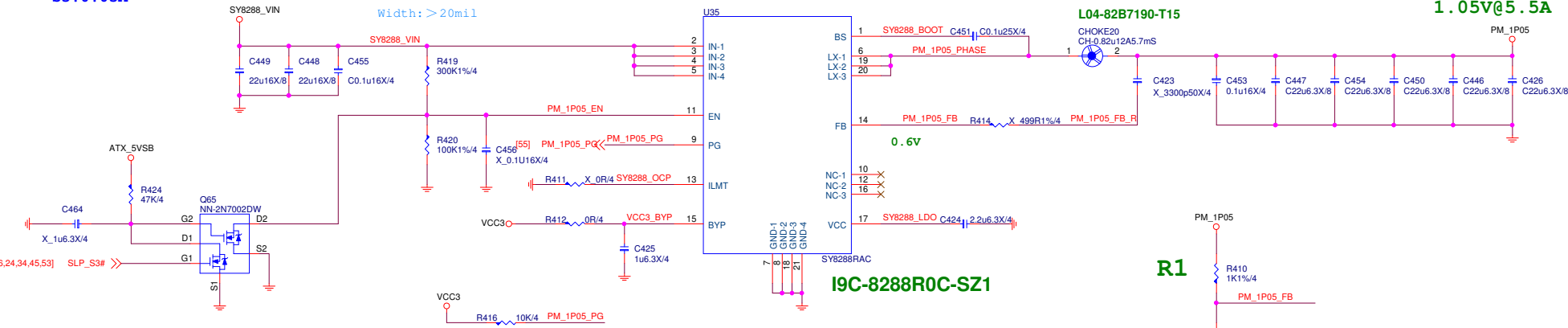
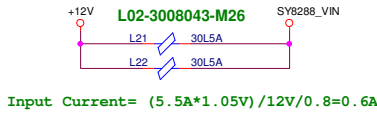
$$= 2.502V$$



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FOR Promontory 1.05V_S0

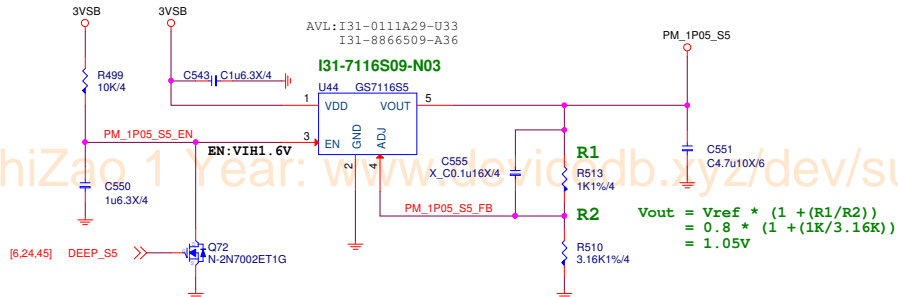
1.05V
S0:5.5A
S5:0.05A



SY8288_OCP	OCP
0	8A
floating	12A
1	16A

FOR Promontory 1.05V_S5

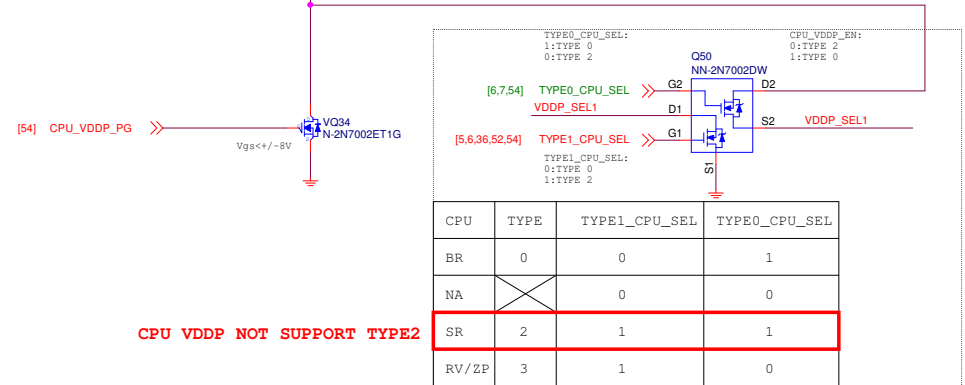
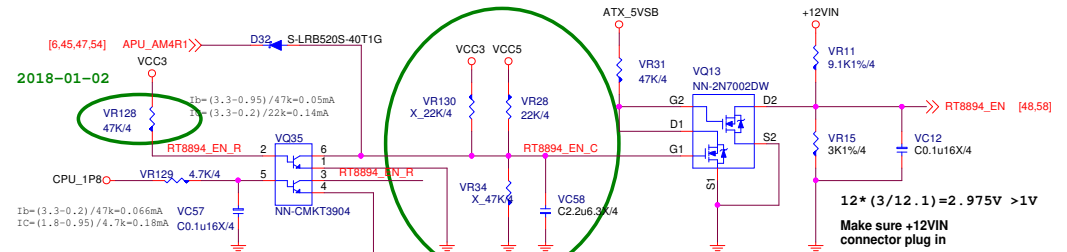
1.05V@0.05A



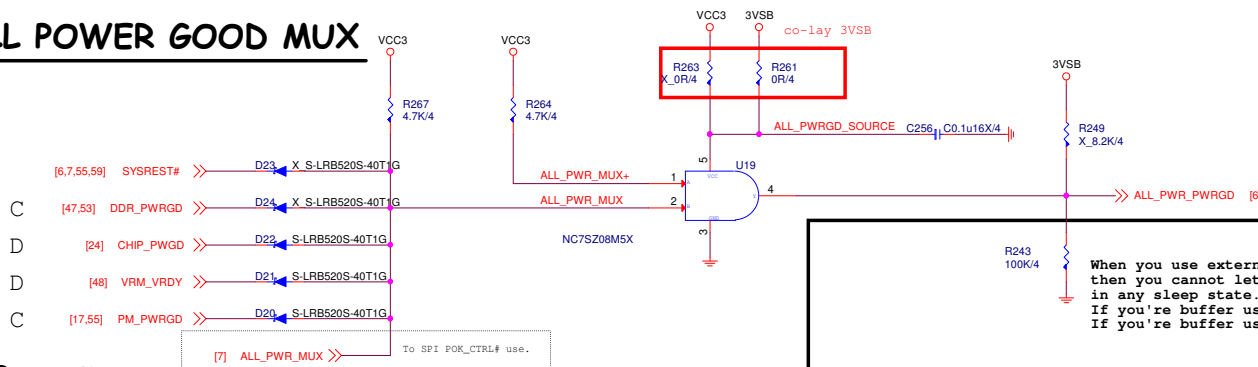
DeviceDB VIP + XinZhiZao 1 Year: www.device-db.xyz/dev/subscriptions/

VRM_Enable circuit

2018-01-02

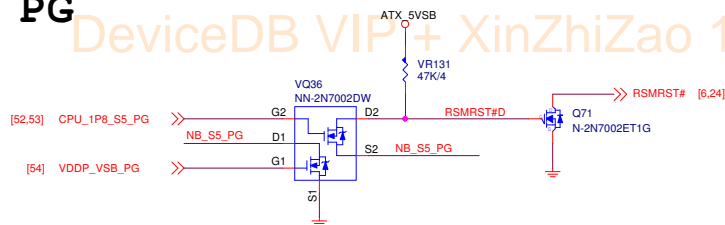


ALL POWER GOOD MUX

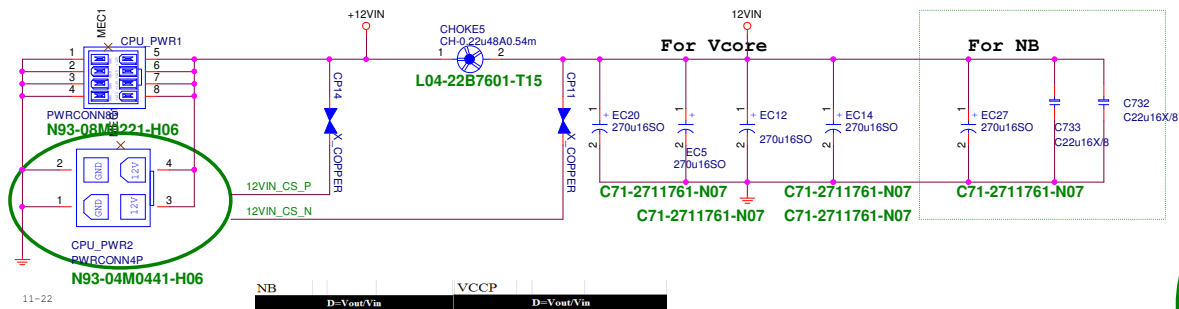


S0 PG

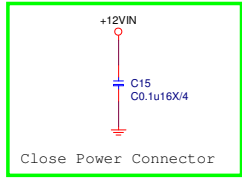
S5 PG



CPU POWER CONNECTOR

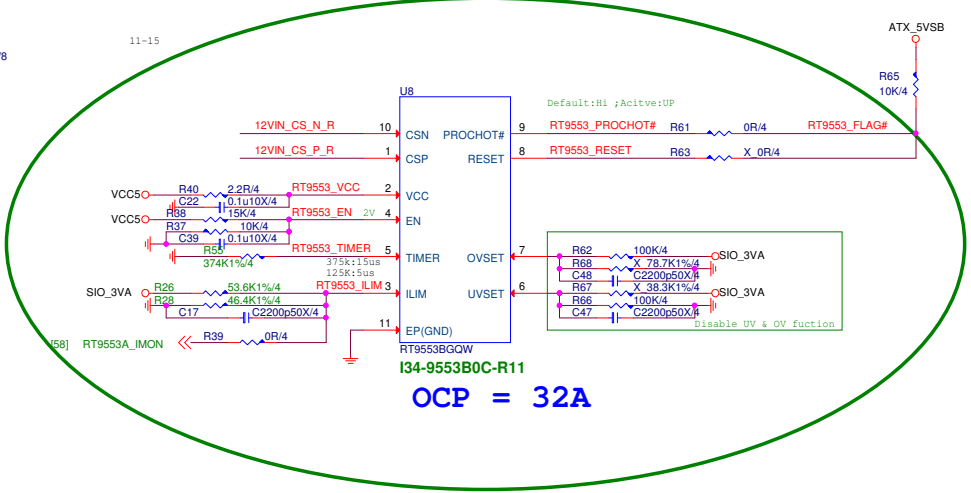


NB		VCCP	
D=Vout/Vin		D=Vout/Vin	
Vin = 12	> input voltage	Vin = 12	> input voltage
Vout = 1.4	> output Vcore	Vout = 1.4	> output Vcore
D = 0.116667		D = 0.116667	
Io = Icoremax*0.8		Io = Icoremax*0.8	
I core(max) = 75	> Vcore current	I core(max) = 125	> Vcore current
I avg = 75	A	I avg = 125	A
I ripple=(Io*sqrt(D*(1-D)))/Phase		I ripple=(Io*sqrt(D*(1-D)))/Phase	
Phase = 2	phase	Phase = 4	phase
I ripple = 12.03835	A	I ripple = 10.03196	A
How many pcs. Of Cap.		How many pcs. Of Cap.	
I ripplecap = 5000 in A		I ripplecap = 5000 in A	
COEtemp = 1		COEtemp = 1	
Input Cap. = 3	pcs.	Input Cap. = 3	pcs.



RT9553B CURRENT SENSE

RT9553 PIN5: When start OV/UV, RESET delay time can meet SPEC 15us.

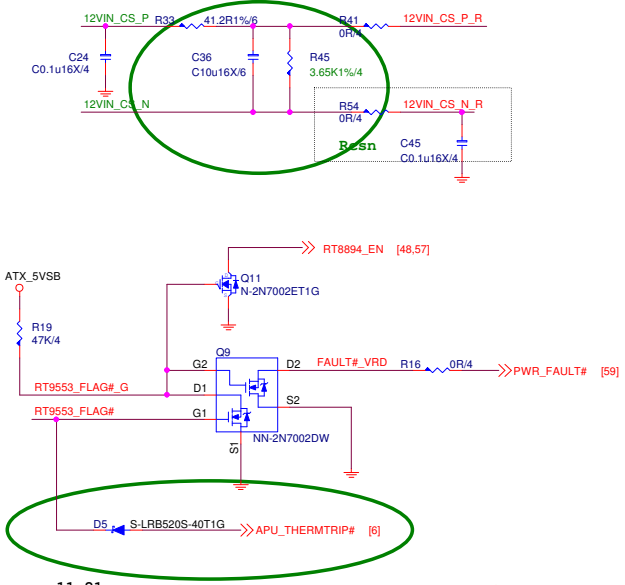
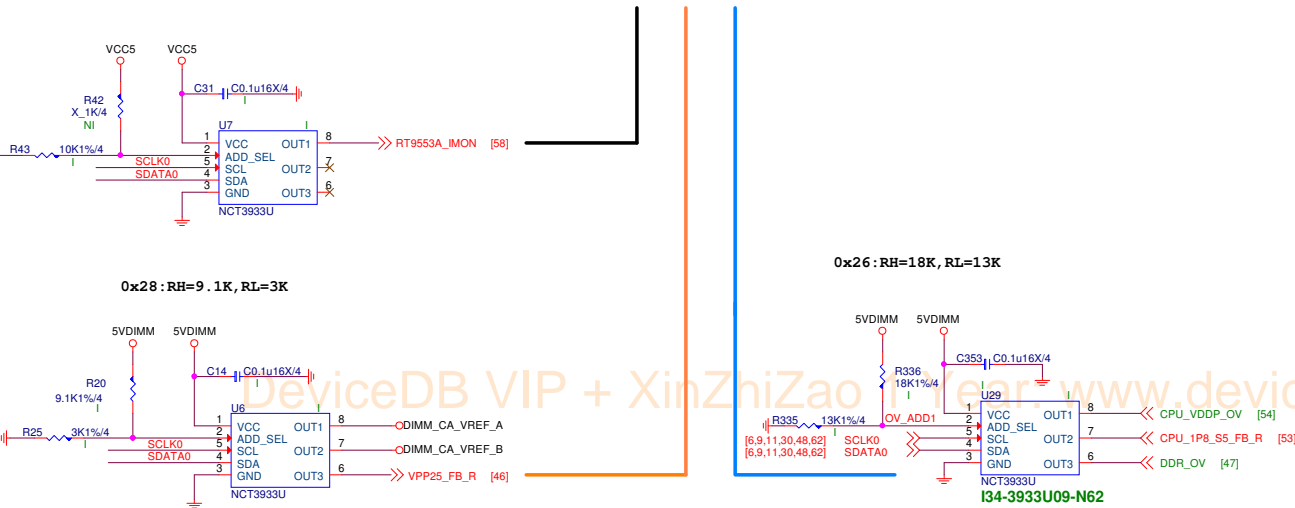


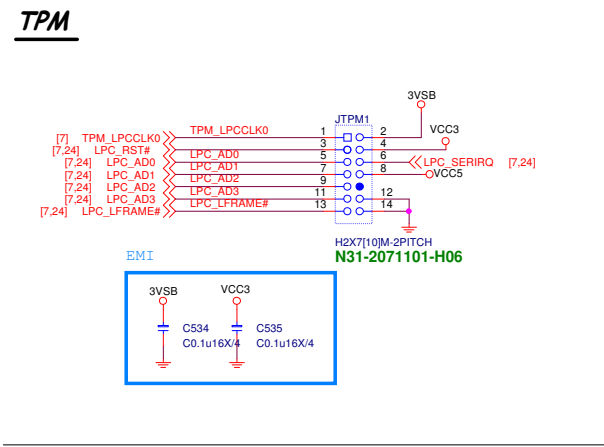
OC = 32A

Over Voltage Control IC

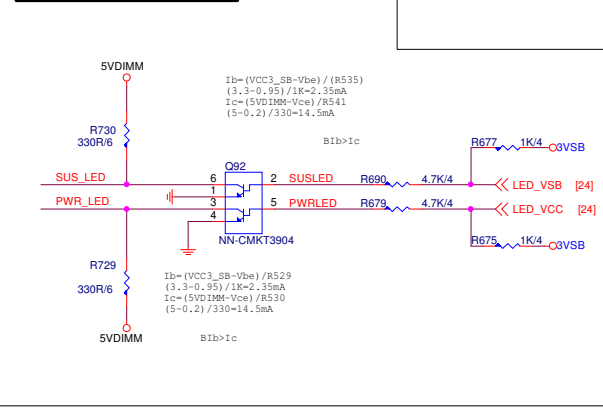
UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0x28	0x26	0x24	0x22	0x20
RH (KOhm)	OPEN	3.9	3	2.2	1.3	10
RL (KOhm)	10	1.3	2.3	3	3.9	OPEN
BUS_SEL	0%	25%	40%	60%	75%	100%



TPM

LED (for NCT6797)



Voltage Measure Point

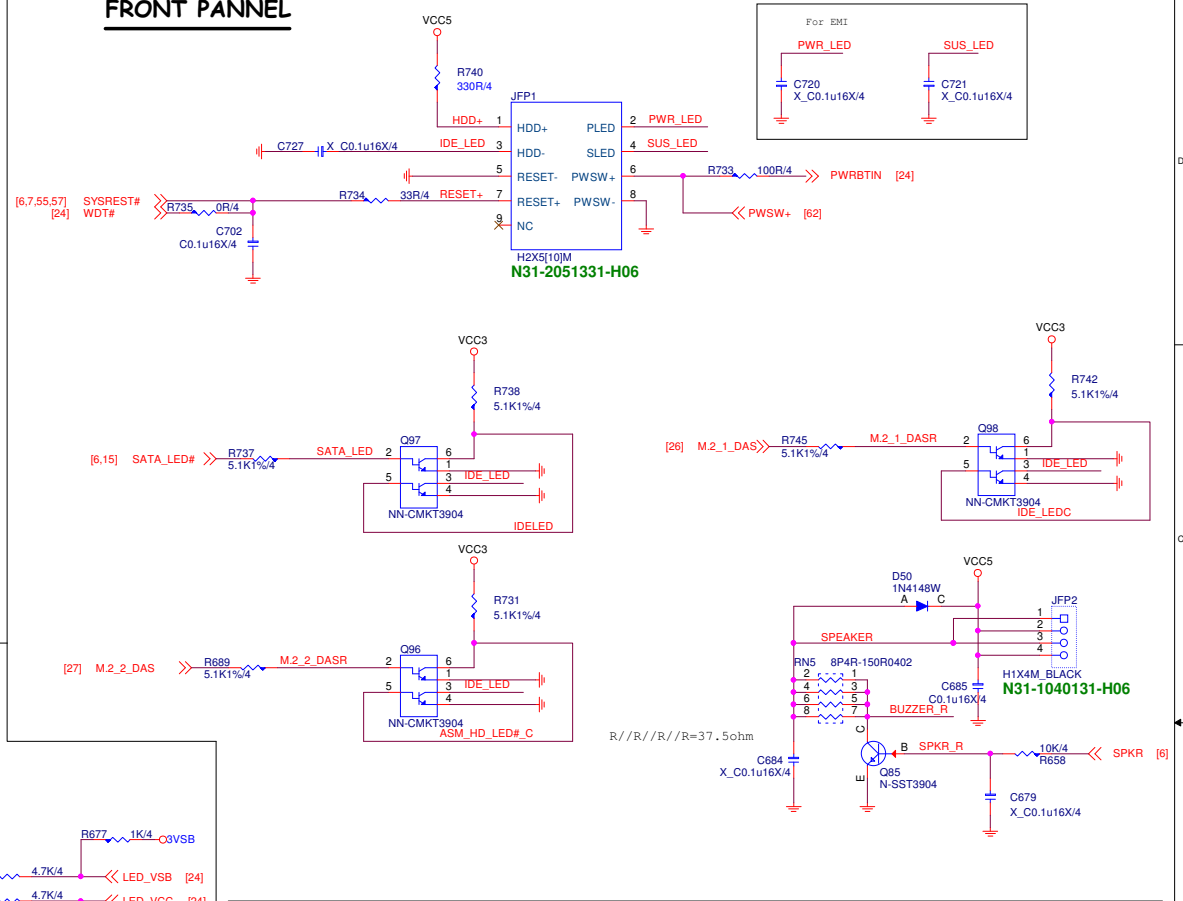



Figure 1-10: Power supply connections for the i.MX6Q. The diagram shows a schematic of the power supply section of the i.MX6Q. It includes connections for VCCP_NBO, CPU_VDDPO, VCC_DDR, VCCORE, +12V, and VCC5. Each connection is shown with a capacitor (C583, C586, C582, C581, C585, C584) and a 10uF 6.3X/6V capacitor. The connections are labeled with a blue circle and a number (1) indicating the connection point. The connections are: VCCP_NBO to TP_CPU_NB, CPU_VDDPO to TP_CPU_VDDP, VCC_DDR to TP_VCC_DDR, VCCORE to TP_CPU_CORE, +12V to TP_+12V, and VCC5 to TP_VCC5.

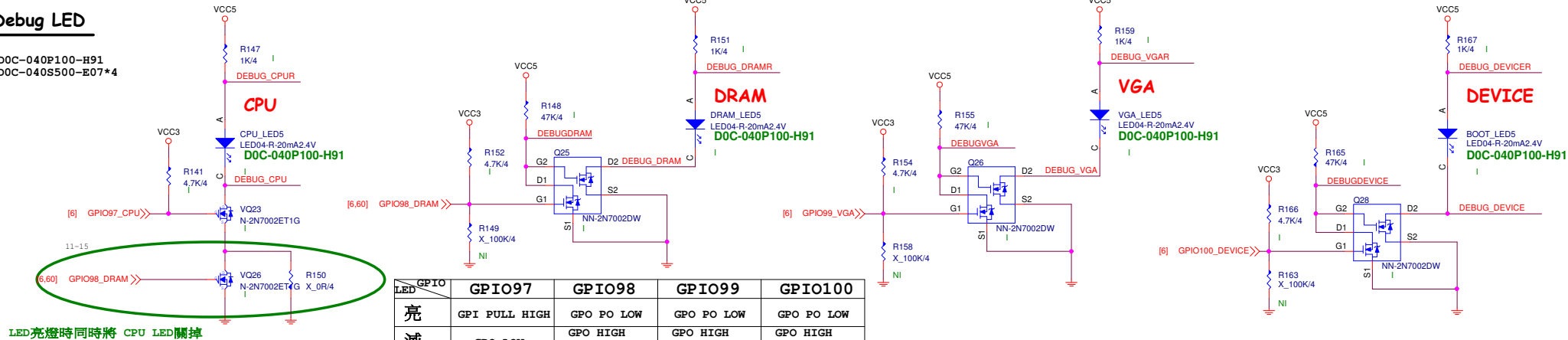
HDMI_PWR_5V	1	TP_HDMI_PWR_5V
DVI_VGA_5V	1	TP_DVI_VGA_5V
USB30_HDMI	1	TP_USB30_HDMI
USB30_VCC2	1	TP_USB30_VCC2
USB30_VCC1	1	TP_USB30_VCC1
USB30_TYPEA	1	TP_USB30_TYPEA
USB30_LAN	1	TP_USB30_LAN
USB_PS2_1	1	TP_USB_PS2_1
USB20_VCC2	1	TP_USB20_VCC2
USB20_VCC1	1	TP_USB20_VCC1
5V_FUSB	1	TP_5V_FUSB
5V_RUSB	1	TP_5V_RUSB
VCC3	1	TP_VCC3
5VDDIM	1	TP_5VDDIM
5VDUAL	1	TP_5VDUAL
3VSB	1	TP_3VSB
ATX_5VSB	1	TP_ATX_5VSB

VTT_DDR0	1	TP_VTT_DDR
VPP25	1	TP_VPP25
CPU_IP8	1	TP_CPU_IP8
CPU_IP8_S5	1	TP_CPU_IP8_S5
PM_IP05	1	TP_PM_IP05
PM_IP05_S5	1	TP_PM_IP05_S5
PM_2P5V	1	TP_PM_2P5V
VCCP_NB_S5	1	TP_VCCP_NB_S5
CPU_VDDP_S5	1	TP_CPU_VDDP_S5
CPU_V_1P5V	1	TP_CPU_V_1P5V

 MSI <small>Micro-Star International, Inc.</small>			
www.msi.com			
Link to the Future			
MICRO-START INT'L CO.,LTD.			
Title ATX/Front Panel			
Size Custom	Document Number MS-7B79		Rev 1.1/2.1
Date: Tuesday, February 13, 2018	Sheet 59	of 72	

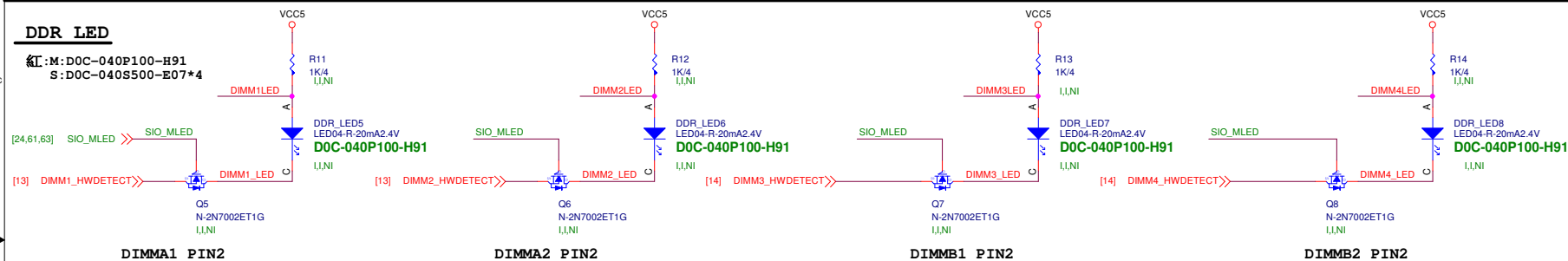
EZ Debug LED

紅:M:D0C-040P100-H91
S:D0C-040S500-E07*4

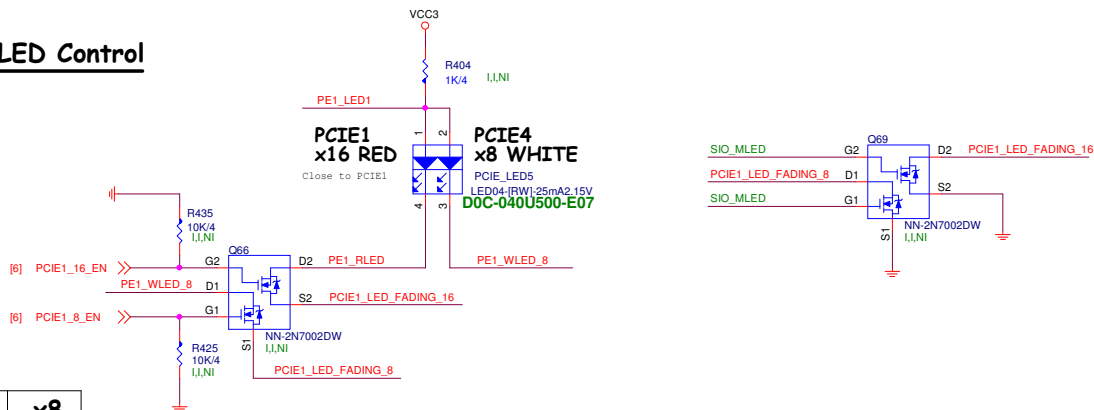


DDR LED

紅:M:D0C-040P100-H91
S:D0C-040S500-E07*4



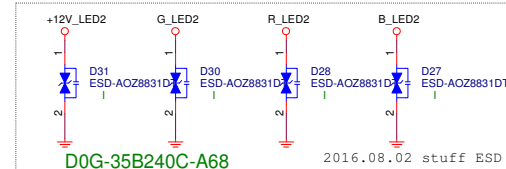
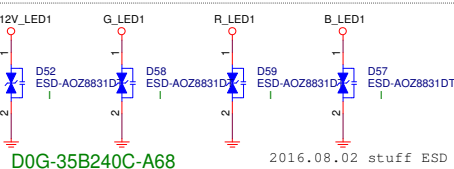
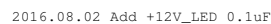
PCI Express LED Control




DeviceDB VIP + XinZhiZao 1 Year: www.device-db.xyz/dev/subscriptions/

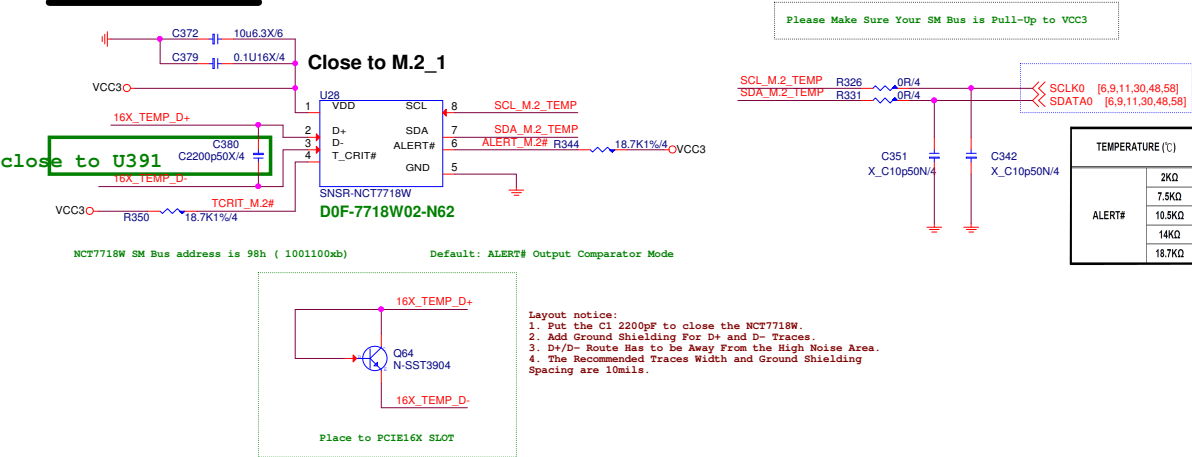
	x16	x8
PCIE1	Red	X
PCIE4	X	White

2016.07.06 Use TPS25944L

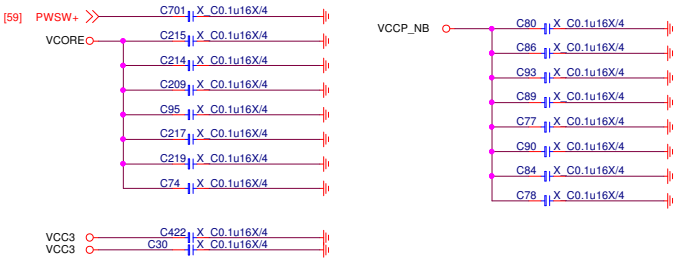
PM SPEC Default WHITE Color

	MSI <small>Micro-Star International, Inc.</small>	<i>Link to the Future</i> MICRO-START INT'L CO.,LTD.
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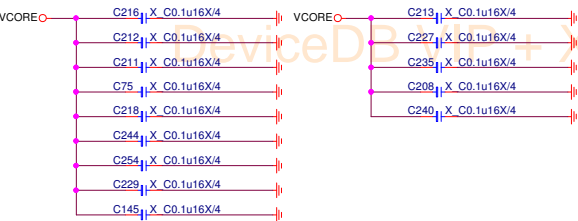
NCT7718W



Add for EMI

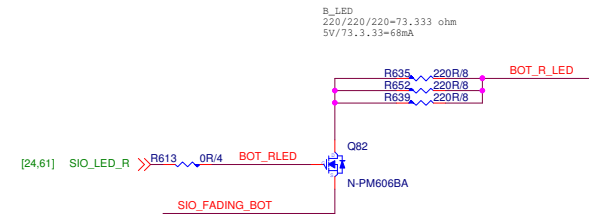
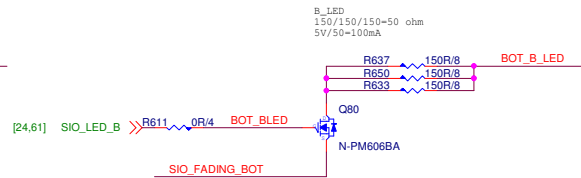
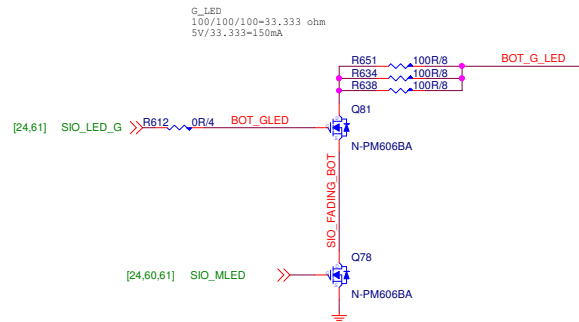
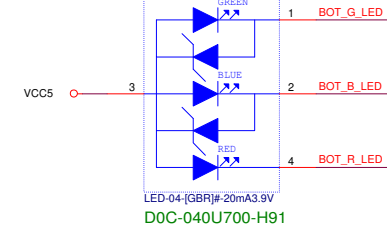
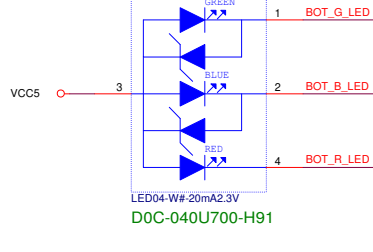
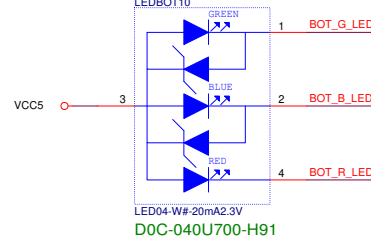
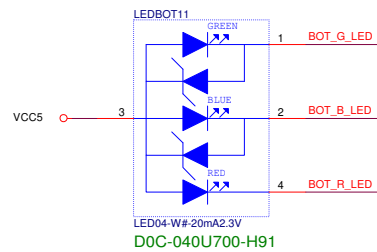
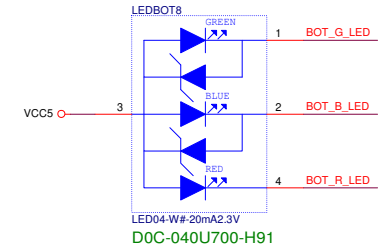
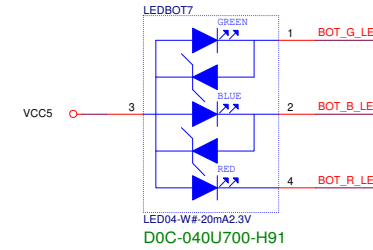
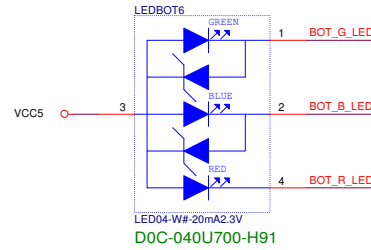
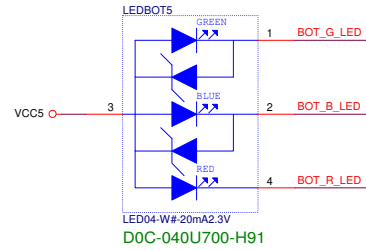


return path



Mystic Light/Right Track LED *8

0.09A*8=0.72A



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OPTION BOM PARTS

60 Level

	A	B	C	D	E
PCIE X16 SLOTT	<div>OPT_PCIE_X16_1</div> <div>PCIE_X16</div> <div>SLOT_PCIEXP164_13</div> <div>N11-1641491-L06</div>	<div>OPT_PCIE_X16_2</div> <div>PCIE_X16</div> <div>SLOT_PCIEXP164_13</div> <div>N11-1641671-L06</div>			<div>OPT_PCIE_X16_3</div> <div>PCIE_X16</div> <div>SLOT_PCIEXP164_13</div> <div>N11-1641671-L06</div>
PCIE X8 SLOTT	<div>OPT_PCIE_X8_1</div> <div>PCIE_X16</div> <div>SLOT_PCIEXP100_5</div> <div>N11-1000221-L06</div>	<div>OPT_PCIE_X8_2</div> <div>PCIE_X16</div> <div>SLOT_PCIEXP100_3</div> <div>N11-1000261-L06</div>	<div>OPT_PCIE_X8_3</div> <div>PCIE_X16</div> <div>SLOT_PCIEXP100_5</div> <div>N11-1000321-L06</div>	<div>OPT_PCIE_X8_4</div> <div>PCIE_X16</div> <div>SLOT_PCIEXP100_3</div> <div>N11-1000231-L06</div>	<div>OPT_PCIE_X8_5</div> <div>PCIE_X16</div> <div>SLOT_PCIEXP100_5</div> <div>N11-1000331-L06</div> <div>FOOTPRINT</div> <div>SLOT_PCIEXP100_5 可包容</div> <div>SLOT_PCIEXP100_3</div>
REAL USB Type A	<div>OPT_USB_A_1</div> <div>BB-TYPE_A</div> <div>鍍金</div> <div>USB_A1_9_USB3_1_1</div> <div>N53-09M0861-L06</div>	<div>OPT_USB_A_2</div> <div>BB-TYPE_A</div> <div>鍍金</div> <div>USB_A1_9_USB3_1_1</div> <div>N53-09M0591-L06</div>	<div>OPT_USB_A_3</div> <div>BB-TYPE_A</div> <div>鍍金</div> <div>USB_A1_9_USB3_1_1</div> <div>N53-09M0671-L06</div>		<div>OPT_USB_A_4</div> <div>BB-TYPE_A</div> <div>鍍金</div> <div>USB_A1_9_USB3_1_1</div> <div>N53-09M0851-L06</div>
SOLID CAP 270u16	<div>OPT_270u16_BLK1</div> <div>60u16_CAP</div> <div>C_P3_5_D8_H8</div> <div>C71-2711761-N07</div>	<div>OPT_270u16_BU1</div> <div>60u16_CAP</div> <div>C_P3_5_D8_H9</div> <div>C71-27117D1-A05</div>			<div>FOOTPRINT</div> <div>C_P3_5_D8_H12 因為機構無法使用 請注意!</div> <div>C_P3_5_D8_H9 可包容</div> <div>C_P3_5_D8_H8</div>
SOLID CAP 560u6.3	<div>OPT_560u6.3_BLK1</div> <div>60u16_CAP</div> <div>C_P2_5_D6_3_H9_5</div> <div>C71-5610671-N07</div>	<div>OPT_560u6.3_BU1</div> <div>60u16_CAP</div> <div>C_P2_5_D6_3_H9</div> <div>C71-56106F1-A05</div>			<div>FOOTPRINT</div> <div>C_P2_5_D6_3_H9_5 可包容</div> <div>C_P2_5_D6_3_H9</div>
SOLID CAP 470u6.3	<div>OPT_470u6.3_BLK1</div> <div>60u16_CAP</div> <div>C_P2_5_D6_3_H9_5</div> <div>C71-47106C1-N07</div>	<div>OPT_470u6.3_BU1</div> <div>60u16_CAP</div> <div>C_P2_5_D6_3_H9</div> <div>C71-47106K1-A05</div>			<div>FOOTPRINT</div> <div>C_P2_5_D6_3_H9_5 可包容</div> <div>C_P2_5_D6_3_H9</div>
SOLID CAP 100u16	<div>OPT_100u16_BLK1</div> <div>60u16_CAP</div> <div>C_P2_5_D6_3_H5</div> <div>C71-10116J1-N07</div>	<div>OPT_100u16_BU1</div> <div>60u16_CAP</div> <div>C_P2_5_D6_3_H6</div> <div>C71-10116Q1-A05</div>			<div>FOOTPRINT</div> <div>C_P2_5_D6_3_H6 可包容</div> <div>C_P2_5_D6_3_H5</div>
MEM SLOTT	<div>OPT_MEM_BLK1</div> <div>MEM_SLOT</div> <div>DDRIV_D288</div> <div>N13-2880581-L06</div>	<div>OPT_MEM_RED1</div> <div>MEM_SLOT</div> <div>DDRIV_D288</div> <div>N13-2880701-L06</div>			<div>OPT_MEM_WHITE1</div> <div>MEM_SLOT</div> <div>DDRIV_D288</div> <div>N13-2880541-L06</div> <div>FOOTPRINT</div> <div>DDRIV_D288_1_T 可包容</div> <div>DDRIV_D288</div>
MKTG Label	<div>OPT_X370_1</div> <div>X370 GAMING</div> <div>G51-M1SPK85-Q13</div>	<div>OPT_B350_1</div> <div>B350 KRAIT GAMING</div> <div>G51-M1SPK86-Q13</div>	<div>OPT_X370_2</div> <div>X370 SLT PLUS</div> <div>G51-M1SPK87-Q13</div>	<div>OPT_X470_1</div> <div>X470 GAMING PRO</div> <div>G51-M1SPM51-Q13</div>	<div>OPT_X470_4</div> <div>X470 GAMING PLUS</div> <div>G51-M1SPM54-Q13</div>
PCH SINK	<div>OPT_PCH_SINK_1</div> <div>MEM_SLOT</div> <div>X470 GAMING PRO</div> <div>E31-0408920-K08</div>	<div>OPT_PCH_SINK_2</div> <div>MEM_SLOT</div> <div>X470 GAMING PLUS</div> <div>E31-0409610-K08</div>		<div>OPT_PCH_SINK_3</div> <div>MEM_SLOT</div> <div>KRAIT</div> <div>E31-0408920-K08</div>	<div>OPT_PCH_SINK_4</div> <div>MEM_SLOT</div> <div>KRAIT</div> <div>E31-0408970-A87</div>
MOSN +IO	<div>OPT_MOSN_IO_1</div> <div>MEM_SLOT</div> <div>KRAIT</div> <div>E31-0504780-K08</div>	<div>OPT_MOSN_IO_2</div> <div>MEM_SLOT</div> <div>PLUS</div> <div>E31-0505660-K08</div>		<div>OPT_MOSN_IO_3</div> <div>MEM_SLOT</div> <div>PRO</div> <div>E31-0504780-K08</div>	<div>OPT_MOSN_IO_4</div> <div>MEM_SLOT</div> <div>PRO</div> <div>E31-0504820-A87</div>
MOSW	<div>OPT_MOSW_1</div> <div>MEM_SLOT</div> <div>KRAIT</div> <div>E31-0504790-K08</div>	<div>OPT_MOSW_2</div> <div>MEM_SLOT</div> <div>PLUS</div> <div>E31-0505650-K08</div>		<div>OPT_MOSW_3</div> <div>MEM_SLOT</div> <div>PRO</div> <div>E31-0504790-K08</div>	<div>OPT_MOSW_4</div> <div>MEM_SLOT</div> <div>PRO</div> <div>E31-0504830-A87</div>
PS2_USB	<div>OPT_PS2_USB_1</div> <div>PS2_USB</div> <div>IOASM_USB DIN14</div> <div>N58-14M0221-H06</div>	<div>OPT_PS2_USB_2</div> <div>PS2_USB</div> <div>IOASM_USB DIN14</div> <div>N58-14M0241-H06</div>			
HDMI_USB	<div>OPT_HDMI_USB_1</div> <div>HDMI_USB</div> <div>IOASM_USB3_HDMI37</div> <div>N58-37M0101-L06</div>	<div>OPT_HDMI_USB_2</div> <div>HDMI_USB</div> <div>IOASM_USB3_HDMI37</div> <div>N58-37M0111-L06</div>			
LAN_USB	<div>OPT_LAN_USB_1</div> <div>LAN_USB</div> <div>IOASM_RJ45_USB_LED32</div> <div>N58-32F0291-F02</div>	<div>OPT_LAN_USB_2</div> <div>LAN_USB</div> <div>IOASM_RJ45_USB_LED32</div> <div>N58-32F0311-F02</div>			

5010 Level

	A	B	C	D	E
FCH	<div>OPT_X470_NB</div> <div>AMD_218-0891008</div> <div>OB1-7B78001-A08</div>	<div>OPT_B350_NB</div> <div>218-0891005-00-RH</div> <div>B01-21808B5-A08</div>			
M.2 SLOTT	<div>OPT_M2_1</div> <div>M2_Rev_B</div> <div>SLOT_NGFFCARD67_31</div> <div>N15-0670820-L06</div>	<div>OPT_M2_2</div> <div>M2_Rev_B</div> <div>SLOT_NGFFCARD67_2</div> <div>N15-0670330-L06</div>	<div>OPT_M2_3</div> <div>M2_Rev_M</div> <div>SLOT_NGFFCARD67_33</div> <div>N15-0670810-L06</div>		<div>FOOTPRINT</div> <div>SLOT_NGFFCARD67_31 可包容</div> <div>SLOT_NGFFCARD67_2</div>
REAL USB Type C	<div>OPT_USBC_1</div> <div>BB-TYPE_C</div> <div>鍍金</div> <div>USB_C1_24_2</div> <div>N53-24M0180-L06</div>	<div>OPT_USBC_2</div> <div>BB-TYPE_C</div> <div>鍍金</div> <div>USB_C1_24_2</div> <div>N53-24M0040-L06</div>			
PCB	<div>OPT_PCB_1</div> <div>PBS</div> <div>Black</div> <div>7B79-10</div> <div>PD0-07B7911-G37</div> <div>PD0-07B7911-E48</div>	<div>OPT_PCB_2</div> <div>PBS</div> <div>Black/WHITE</div> <div>7B79-20</div> <div>PD0-07B7921-G37</div> <div>PD0-07B7921-E48</div>	<div>OPT_PCB_3</div> <div>PBS</div> <div>Black/Red</div> <div>7A33-31</div> <div>PD0-07A3331-G37</div> <div>PD0-07A3331-E48</div>		
0 Ohm (0402)	<div>OPT_0OHM_5010_1</div> <div>0402-0402</div> <div>5010_0402</div> <div>R11-0000012-W08</div>				
LED	<div>OPT_RED_LED_5010_1</div> <div>RED_LED</div> <div>LED04-R-20mA2_4V_1608-HF</div> <div>D0C-040P100-H91</div>				

5020 Level

	A	B	C	D	E
LED	<div>OPT_RED_LED_5020_1</div> <div>RED_LED</div> <div>LED04-[BR]25mA2.35V_1711-RH</div> <div>5020_0402</div> <div>D0C-040S600-E07</div>				

60 Level

	A	B	C	D	E
Audio cover	<div>OPT_AUD_COV_1</div> <div>AUDIO_COVER</div> <div>AUDIO_COVER_20X19_5</div> <div>E21-7A59010-A91</div>			<div>OPT_AUD_COV_2</div> <div>AUDIO_COVER</div> <div>AUDIO_COVER_20X19_5</div> <div>E21-7A62010-A91</div>	
Audio Jack	<div>OPT_AUD_JACK_1</div> <div>AUDIO_JACK</div> <div>JACK_AUD_D26P</div> <div>N54-26F0351-L06</div>			<div>OPT_AUD_JACK_2</div> <div>AUDIO_JACK</div> <div>AUDIO_JACK6_26P_U2</div> <div>N54-26F0361-L06</div>	
M.2 SCREW	<div>OPT_M2_SCR_1</div> <div>M2_SCR</div> <div>SCREW</div> <div>E2B-7A69010-A89</div>				
PCIE X4 SLOTT	<div>OPT_PCIE_X4_1</div> <div>PCIE_X16</div> <div>SLOT_PCIEXP100_5</div> <div>N11-1000221-L06</div>	<div>OPT_PCIE_X4_2</div> <div>PCIE_X16</div> <div>SLOT_PCIEXP100_5</div> <div>N11-1000261-L06</div>	<div>OPT_PCIE_X4_3</div> <div>PCIE_X16</div> <div>SLOT_PCIEXP100_5</div> <div>N11-1000321-L06</div>	<div>OPT_PCIE_X4_4</div> <div>PCIE_X16</div> <div>SLOT_PCIEXP100_5</div> <div>N11-1000331-L06</div>	

MSI

Link to the Future

MICRO-START INT'L CO.,LTD.

Title

BOM Option

Size

Custom

Document Number

MS-7B79

Rev

1.1/2.1

Date:

Tuesday, February 13, 2018

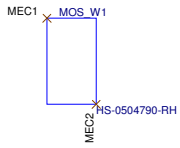
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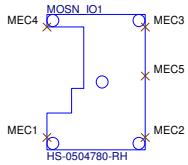
of

72

MOS SINK



E31-0504790-K08



E31-0504780-K08

MANUAL PART



AVL1:
D06-0100161-F52
D06-0100101-K26



OPT_A,A,B

7B79-10
PD0-07B7910-G37, 精成-深圳, 1, 台北微星廠 (MSI)
PD0-07B7910-E48, 競華, 1, 台北微星廠 (MSI)

BIOS LABEL



G51-M1SPXXA-A09

MKTG name Label

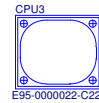


DDR Cover

11-16

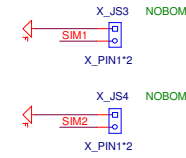
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CPU Socket

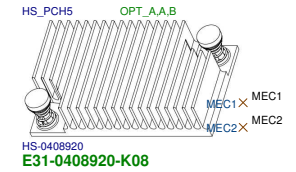


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Simulation

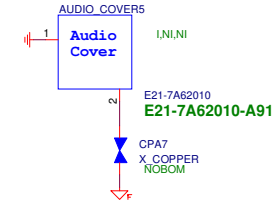


PCH SINK



E31-0408920-K08

AUDIO COVER



ROYALTY

HDMI_LA1
Y01-RHDMI03-000

cFosSoftware I,I,N I GAMING Only

Y02-MU00170-CFO

NAHIMIC I,I,N I

Y02-MU00100-NAH

NVIDIA_SLI I,I,I I

Y01-RNVIDIK-000

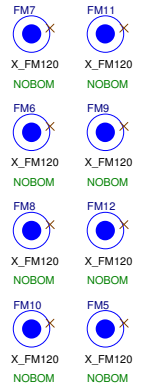
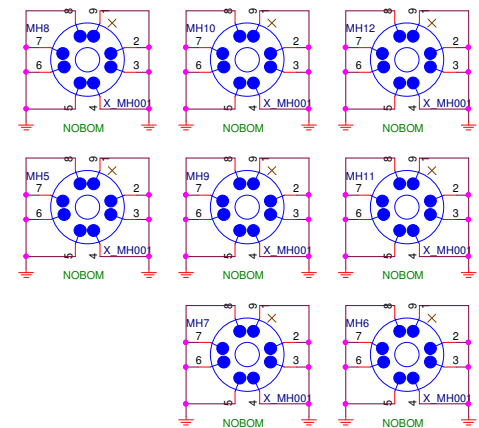
XSPLIT I,I,N I

Y02-MA00401-XSP

SSE I,I,N I

Y02-MA00101-SSE

Optics Orientation Holes



DeviceDB VIP + XinZhiZao 1 Year: www.device-db.xyz/dev/subscriptions/

Schematic Cfg	Project
CFG1-7A33-0A-X370-GAMING_601-7A33-A01	V A
CFG2-7A33-0A-B350-GAMING_601-7A33-A02	V B
CFG3-7A33-0A-X370-SLI PLUS_601-7A33-B01	V C

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Manual Parts			
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